

Exploring the Hardware-Software Interface using an FPGA-based Research Platform



UNIVERSITY OF
CAMBRIDGE

Computer Laboratory

Robert Norton and Simon Moore

Motivation Research into computer architectures is inhibited by the prohibitive cost of making custom hardware and the inadequacies of simulation. Meanwhile, commercial architectures are required to maintain backwards compatibility due to network economics. Therefore computer architectures evolve only very slowly and systems programmers tend to view them as static, meaning that opportunities for interface improvements go unexplored. What is needed is a platform to allow simultaneous evolution of hardware and software, providing a complete OS stack on readily available and affordable, customisable hardware.



Figure 1: FreeBSD running on BERI on DE4 board

Research Platform

BERI (BlueSpec Extensible RISC Implementation) is a 64-bit MIPS-compatible soft processor written in BlueSpec Verilog. It is being developed as part of the CTSRD project. We have synthesised this for Altera's DE4 FPGA development board and successfully ported FreeBSD to it (Figure 1). This provides a complete platform for joint OS and hardware research. We intend to use this platform to challenge current assumptions about the hardware-software interface, demonstrating new architectural features and how they can improve the security and efficiency of the system. For example:

Research Area 1 - Fine Grained Memory Protection

CHERI (Capability Hardware Enhanced RISC Implementation) is a version of BERI with added support for hardware 'capabilities'. These provide a mechanism for fine grained memory protection and an efficient model for privilege escalation, without incurring the costs associated with repeated address space switching when using a traditional TLB for protection. Figure 2 shows the structure of the capability registers, including the 'otype' field which can be used for secure object invocation.

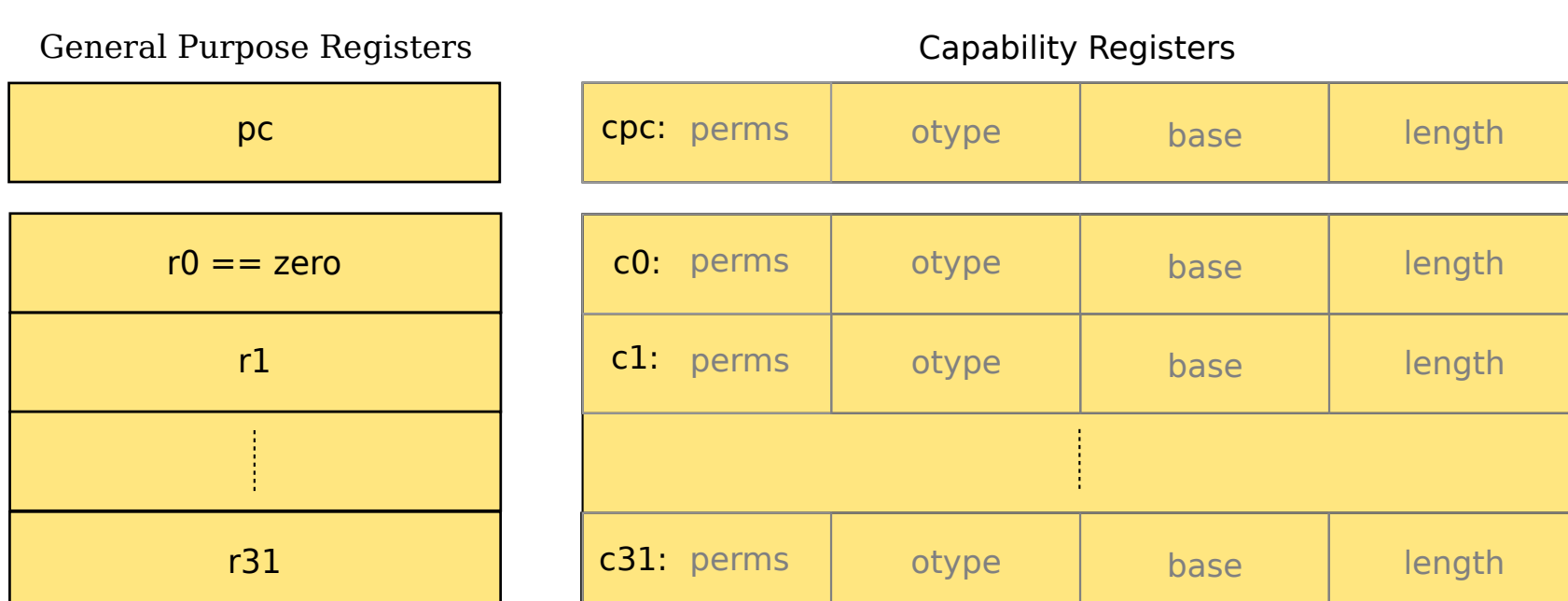


Figure 2: CHERI Registers

Research Area 2 - Multi-Thread/Multi-Core processor with Efficient Inter-Thread Communications

One common approach to exposing more hardware parallelism is multi-threading. By replicating the register file multiple threads of execution can run simultaneously, sharing the hardware resources (Figure 3). The advantage of this is that interleaving instructions from different threads can mask unavoidable delays in single-threaded code, such as load latencies. I have extended BERI to support eight hardware threads which, in addition to providing the performance advantages of multi-threading, can alternatively be used to emulate 8 single threaded processors running at one eighth of the speed. I intend to use this version of the processor to investigate new inter-core communication mechanisms such as asynchronous remote stores, as proposed by Meredydd Luff (Figure 4). I hypothesise that I will be able to demonstrate considerable performance advantages for a parallel language runtime using these new features.

Figure 3:
Multi-threaded
BERI Pipeline

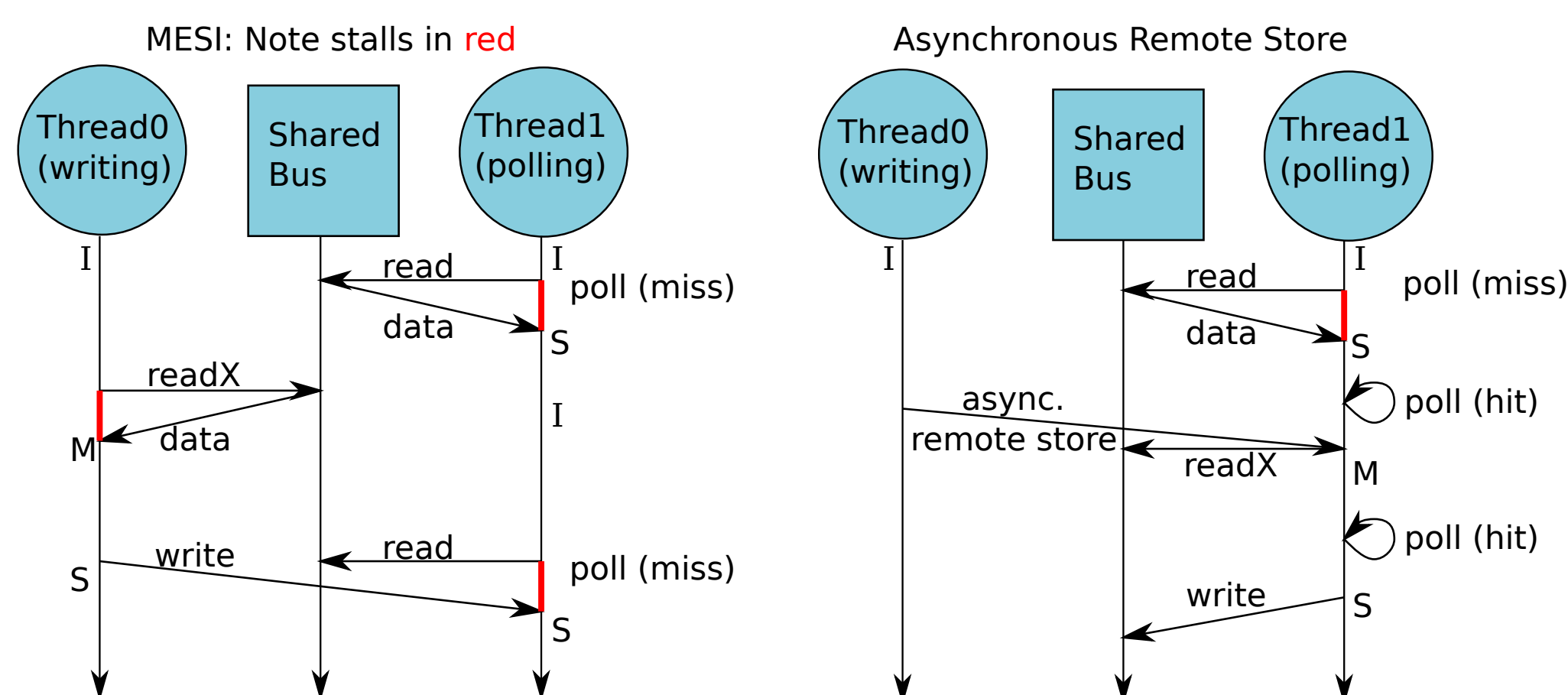
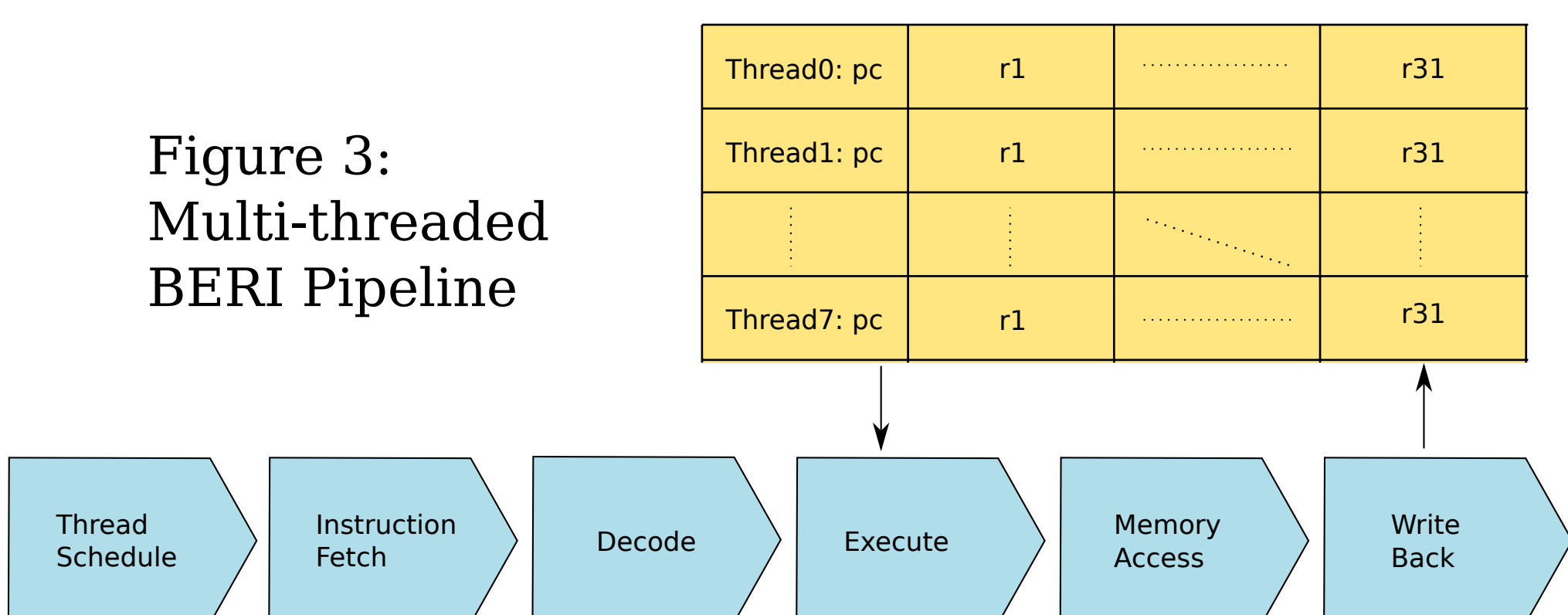


Figure 4: Writing shared flag with MESI cache coherence vs. MESI + asynchronous remote store

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Approved for public release. The BERI/CHERI research platform is sponsored by the Defense Advanced Research Projects Agency (DARPA) and the Air Force Research Laboratory (AFRL), under contract FA8750-10-C-0237. The views, opinions, and/or findings contained in this article/presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.