Programmable Memory Controller for Vector System-on-Chip

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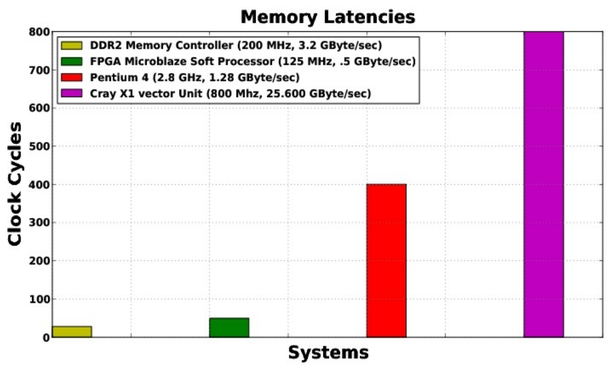
Problem-Formulation

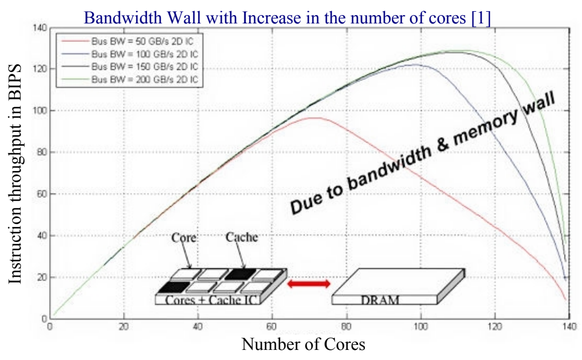
Wall Clock Time increases with the increase of memory size:

`WCT = Number of Cycle / Frequency of CPU`

Number of Clocks are dependent:

- Computation Delay
- Address/Data Management Delay
- On-chip/Off-chip Bus Delay
- Memories Delay



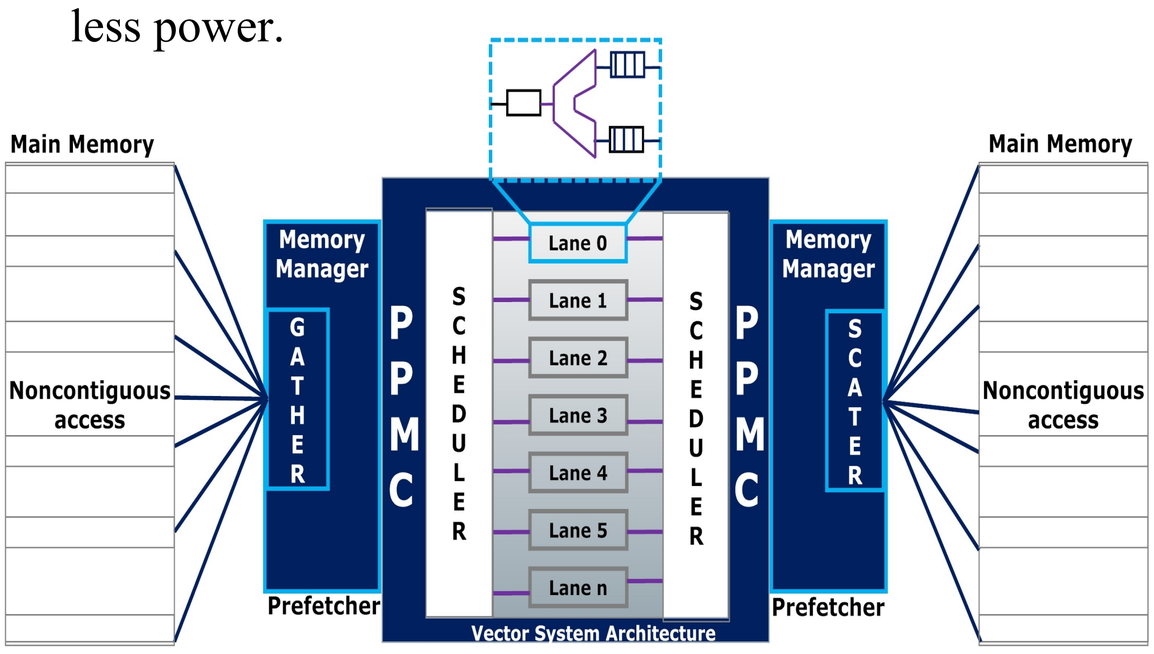


- Efficient memory hierarchy between the computing unit and the DRAM memory.
- Memory access policies, strided scatter/gather prefetchers.
- A programming model is required for the design

Proposal

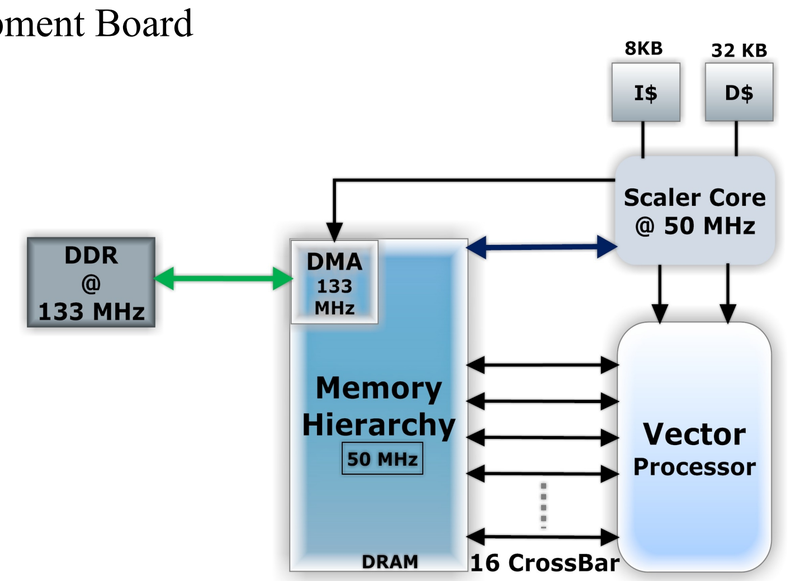
As with conventional scalar processors, all classes of vector machine are required to have a Programmable Memory Controller which includes:

- Manage processing elements without the support of Master core.
- Intelligently schedules multiple data accesses from different threads.
- Efficiently prefetch complex/irregular patterns.
- Support standard C/C++ language calls to identify tasks in software.
- Combine all the functions into one chip the FPGA based system becomes smaller, faster, and consume less power.



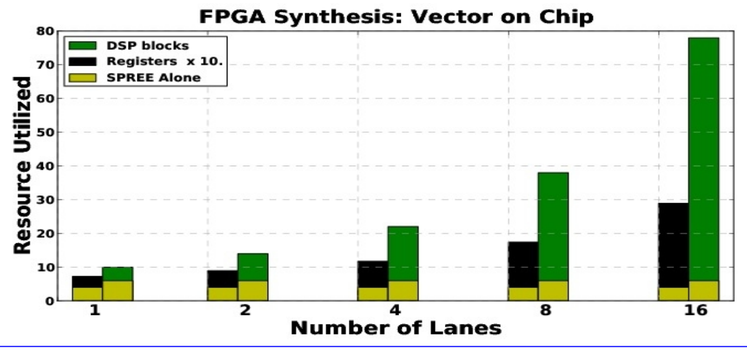
Evaluation

- **Software Compilation Framework**
  - GNU GCC 4.2.0
- **RTL simulation**
  - Modelsim SE version 6.3c
- **FPGA CAD Software**
  - Quartus II
- **Hardware Platform**
  - AlteraDE4 Development Board
- **Application Kernels**
  - Image Processing
  - 2D Filter



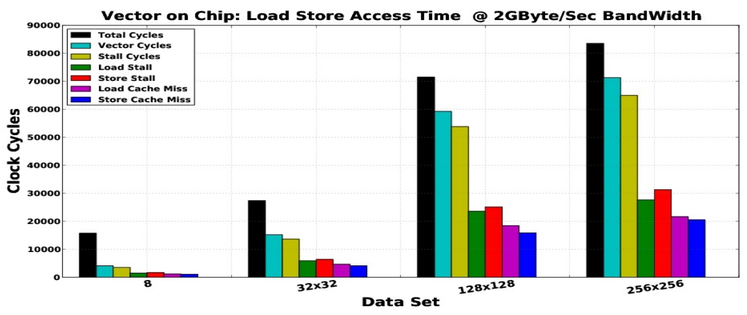
Preliminary Results

Quratus II Synthesis Summary

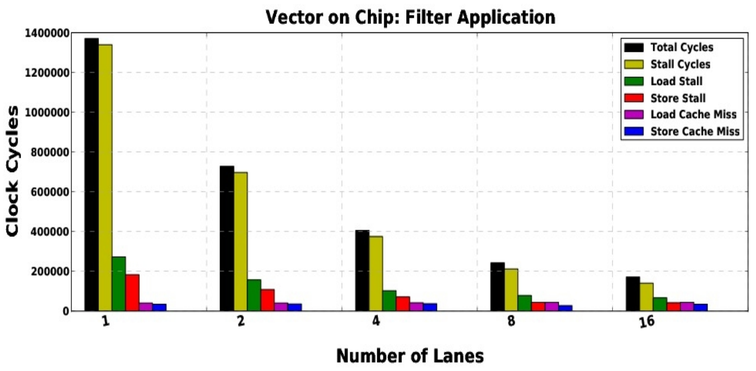


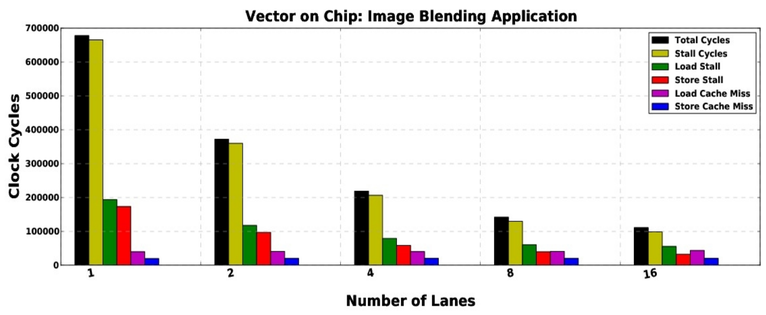
- 64 Maximum Vector Length
- 32-bit (4-byte) Vector Lane Width

Datasets Load/Store Time



Application Execution Time





Conclusions & future work

In future, we are planning to embed a selective static/dynamic set of data access pattern inside Memory Controller for vector accelerator architecture that would effectively eliminate the requirement of programming system by the user for a range of applications.

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- PPMC : A Programmable Pattern based Memory Controller Hussain TASSADAQ,Muhammad Shafiq, Miquel Pericas, Nacho Navarro, Eduard Ayguade ARC 2012, the 8th International Symposium on Applied Reconfigurable Computing 21 - 23 March 2012 The Chinese University of Hong Kong, CUHK, Hong Kong
- PPMC : Hardware Scheduling and Memory Management support for Multi Hardware Accelerators Hussain TASSADAQ, Miquel Pericas, Nacho Navarro, Eduard Ayguade. FPL2012 | 22nd International Conference on Field Programmable Logic and Applications FPL2012 Oslo, Norway, Aug. 29-31, 2012.

[1] Muhammad Bakir; Georgia Tech.