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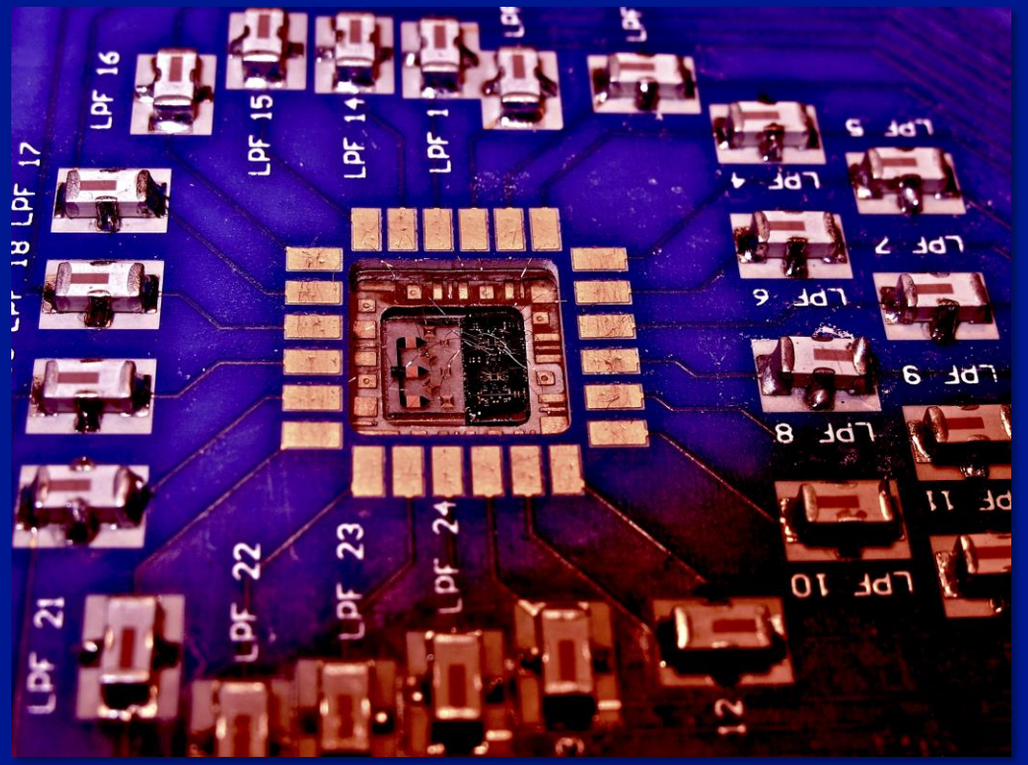


Towards Control of a Large-Scale Quantum Computer

David Reilly

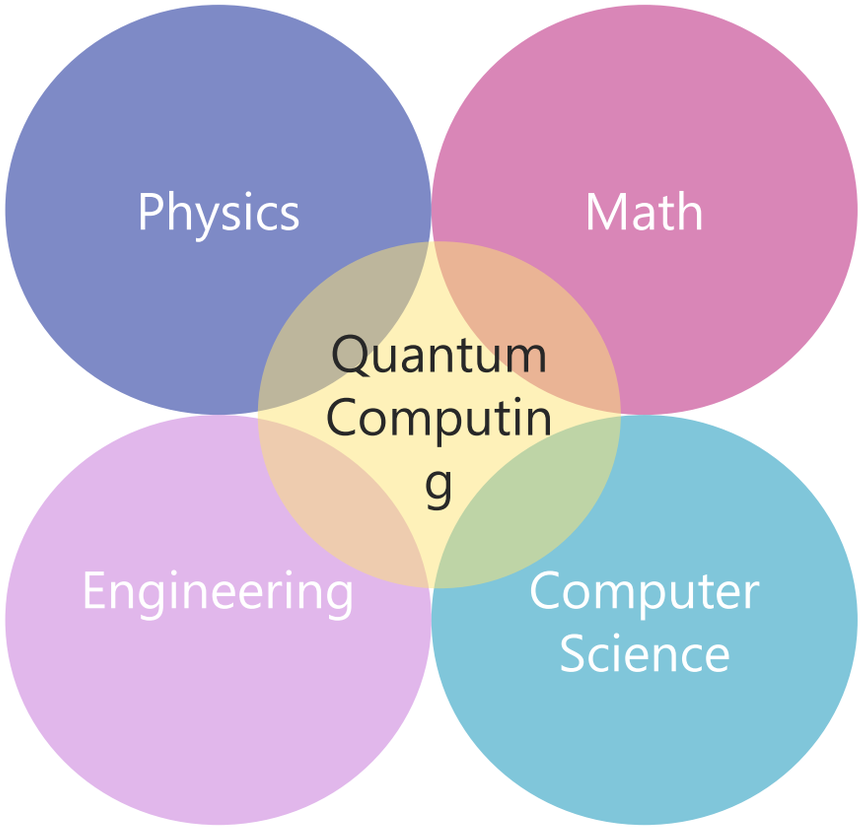
eQus

Australian Government
Australian Research Council

THE UNIVERSITY OF SYDNEY

Microsoft

Multidisciplinary Research



....the rest is just engineering

Is it too early to worry about controlling a quantum computer?

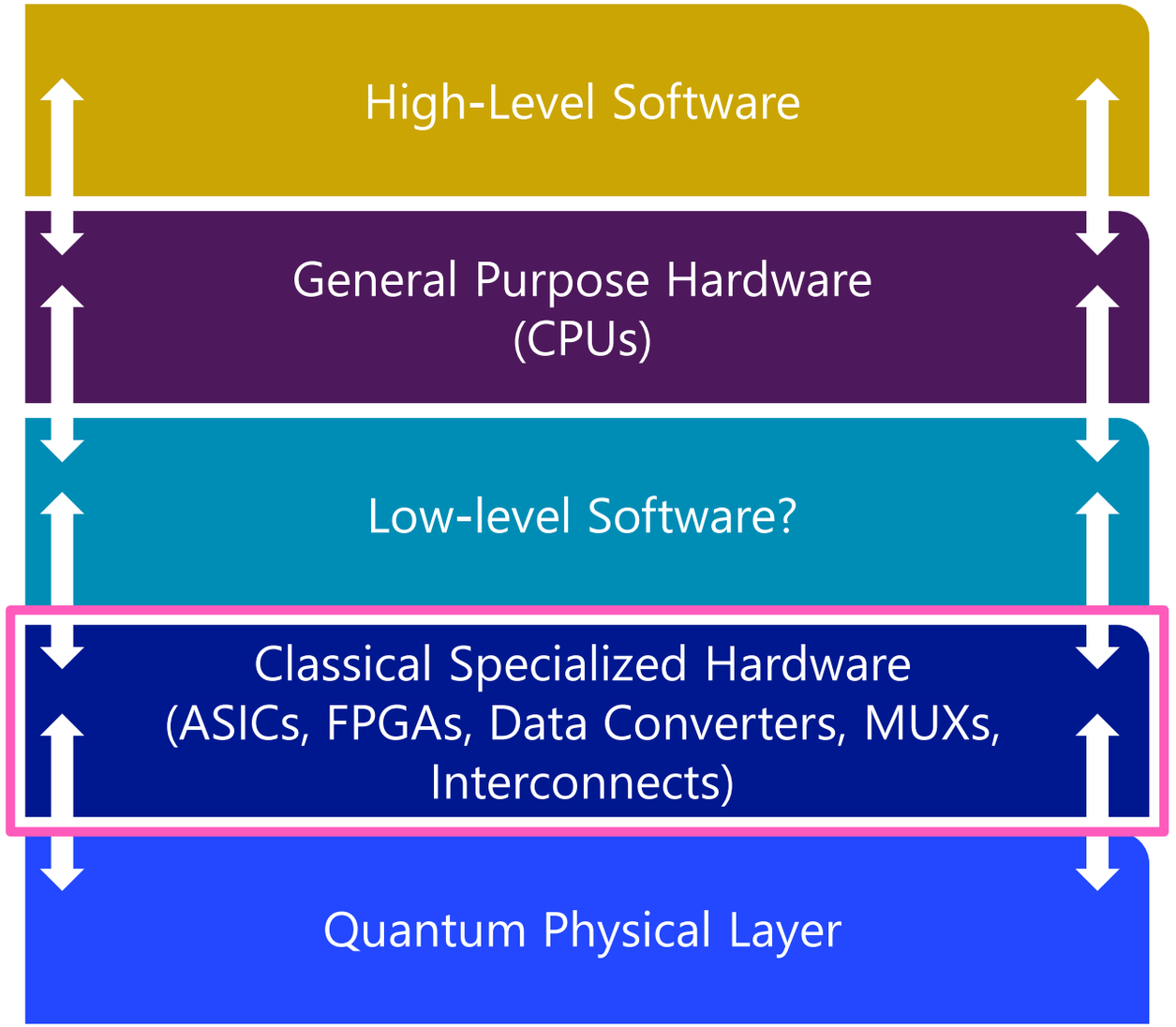
** Which qubit flavors are best suited to today's and tomorrow's classical hardware?*

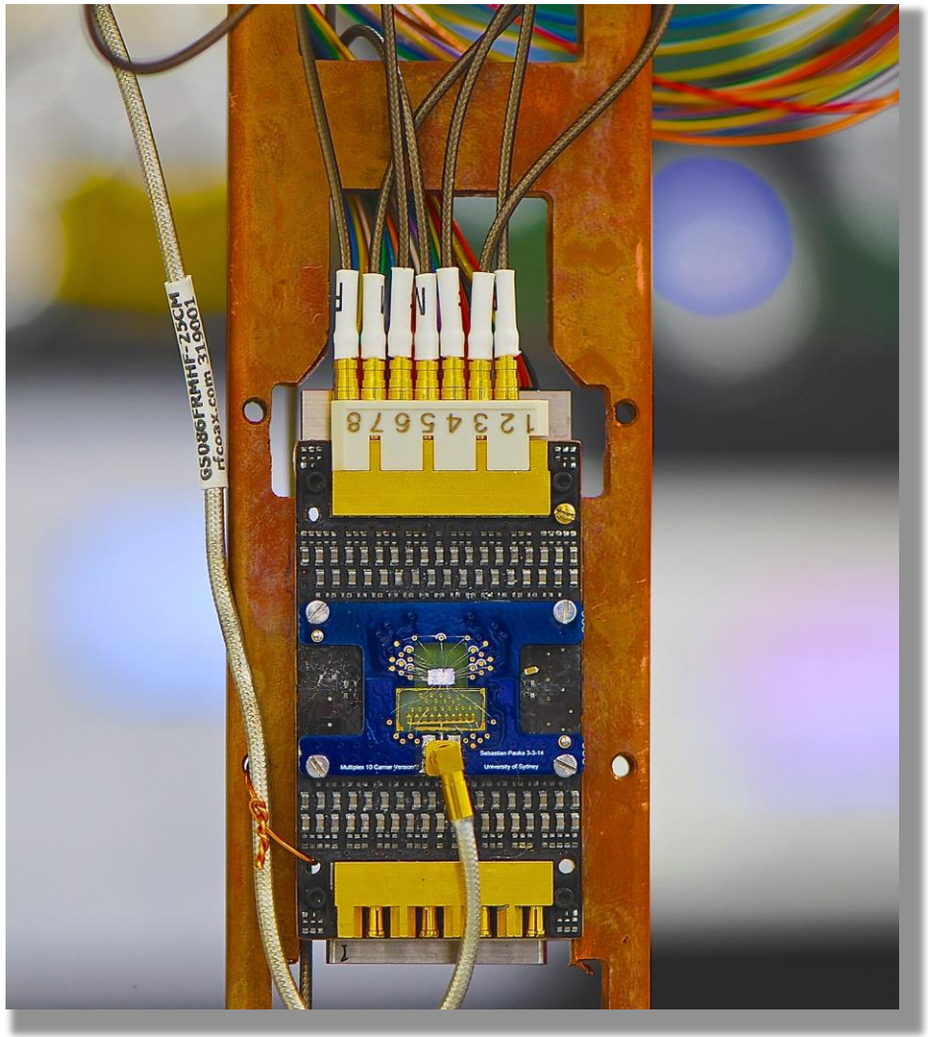
** New physics is possible using very fast, autonomous readout and control, eg, feedback protocols that use adaptive measurements, or quantum error correction.*

** Simple quantum systems are already becoming too complex and tedious for all-human operation, eg, tuning multiple quantum dots.*

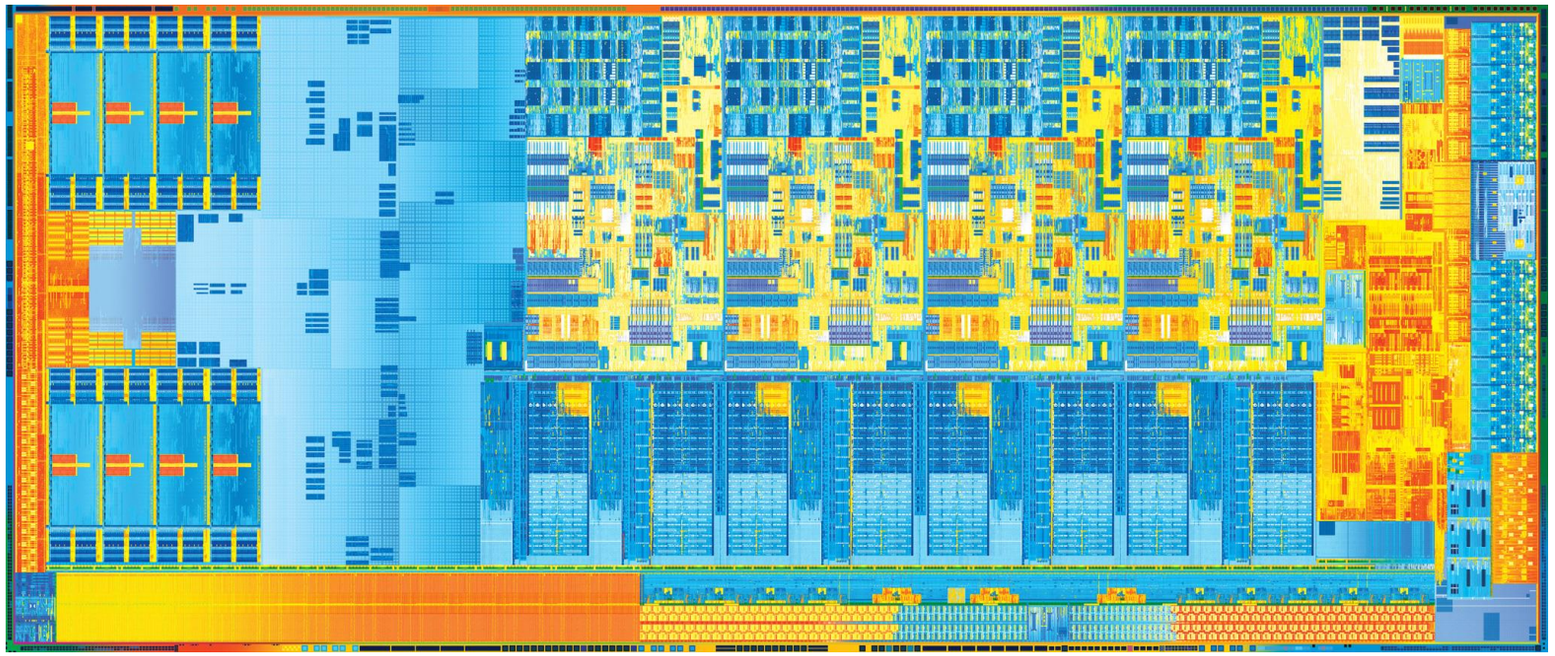
** What are the issues? Where are new developments needed?*

What's there to control?





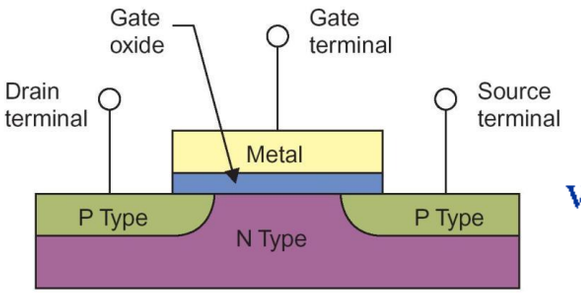
Classical Computation

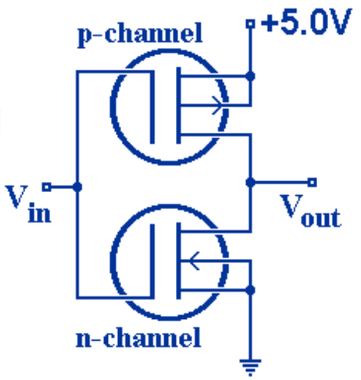


Intel Ivy Bridge: 1.4 Billion transistors on a chip
22 nm feature size, 4 GHz clock.

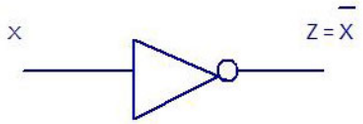
On planet Earth, 10 billion transistors are created every second

Logic operations are implemented with physical circuits (MOSFETs).





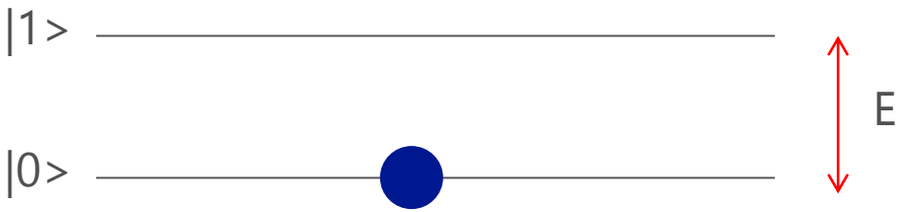
NOT Gate

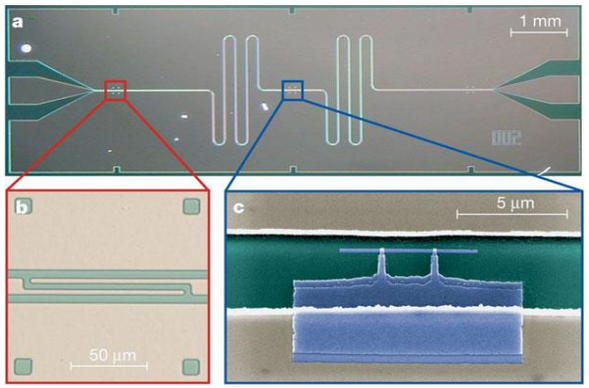


TRUTH TABLE

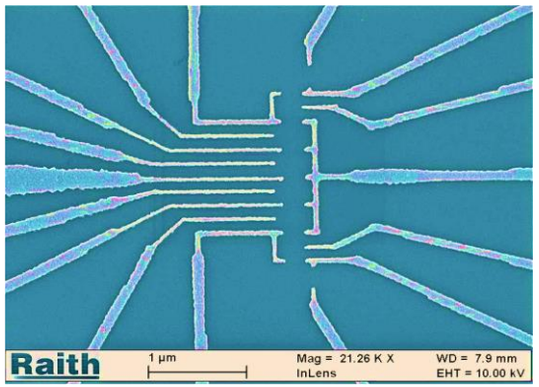
INPUT	OUTPUT
X	Z
0	1
1	0

Quantum Computation

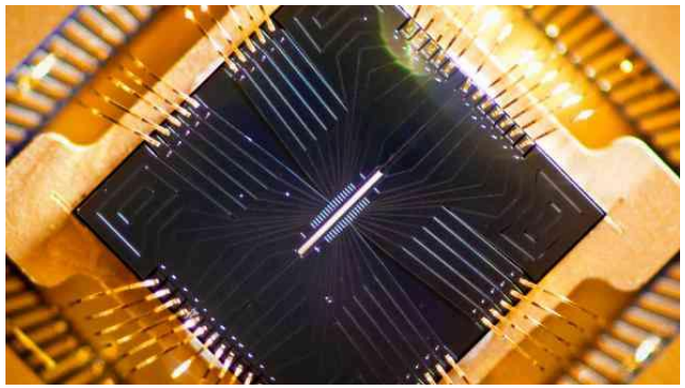




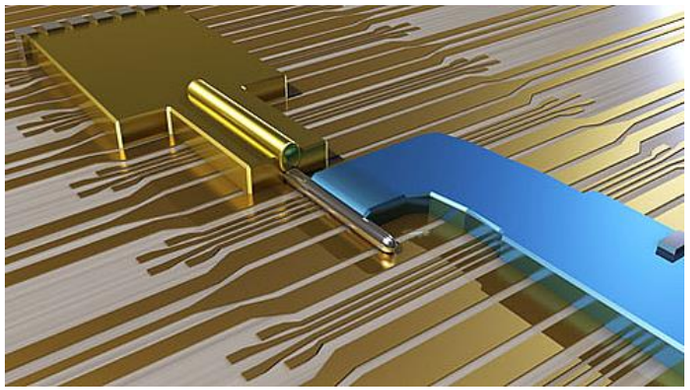
Superconducting Qubits (Yale)



Electron Spin Qubits (Sydney)

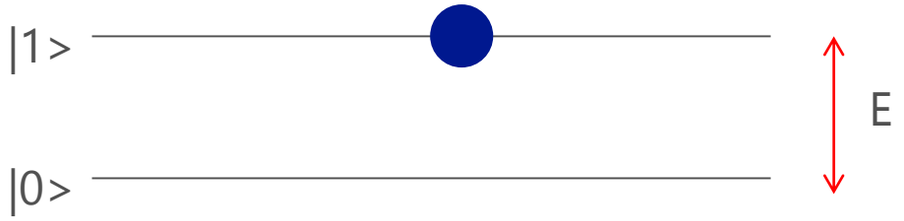


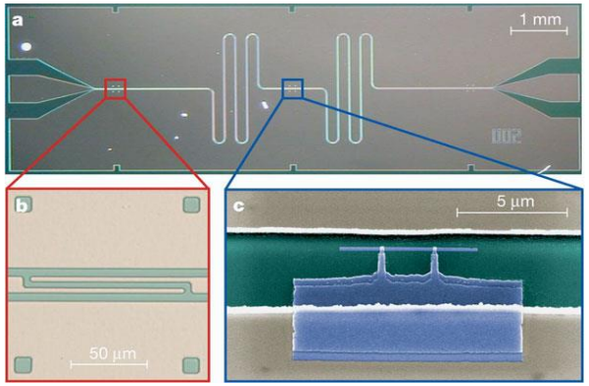
Surface Ion trap (Sandia)

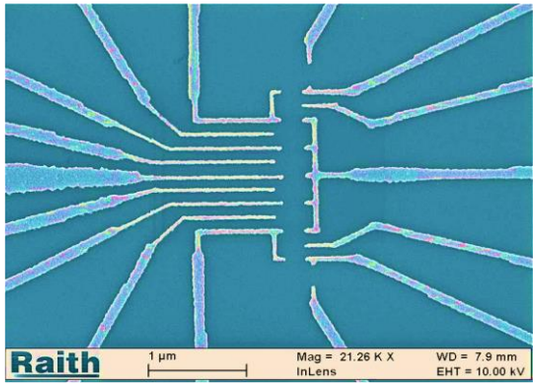


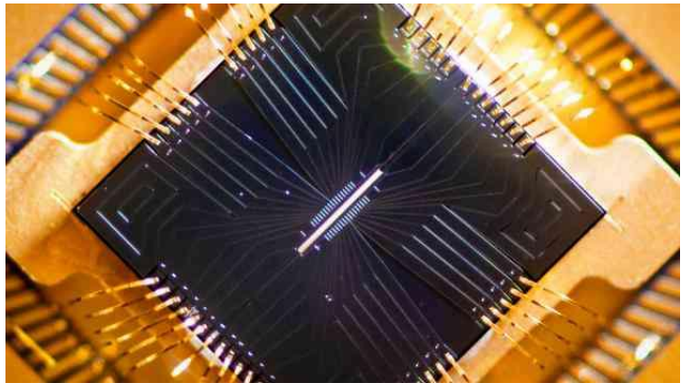
Majorana Qubits (Delft)

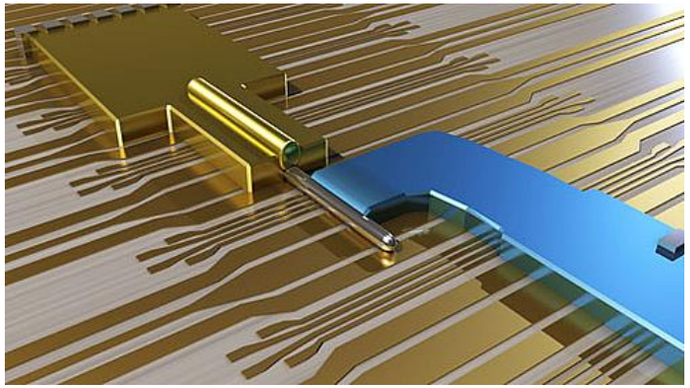
Quantum Control

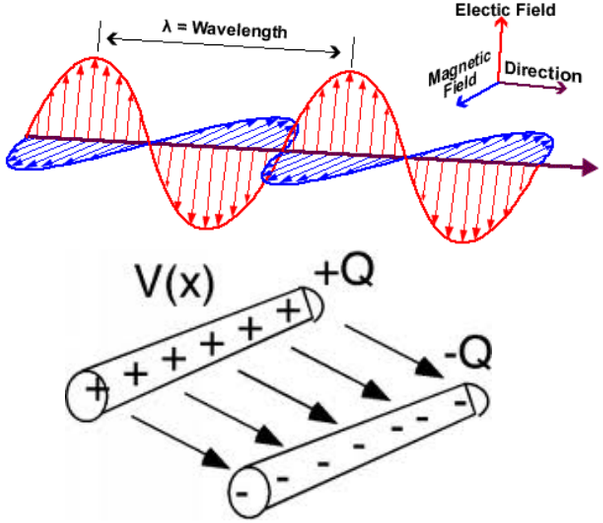


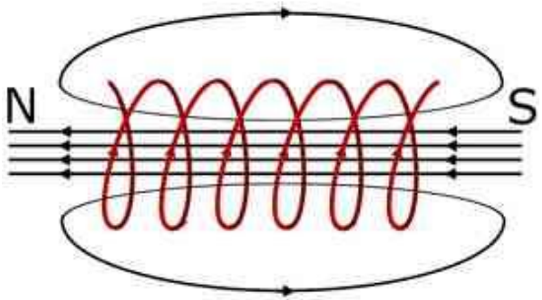


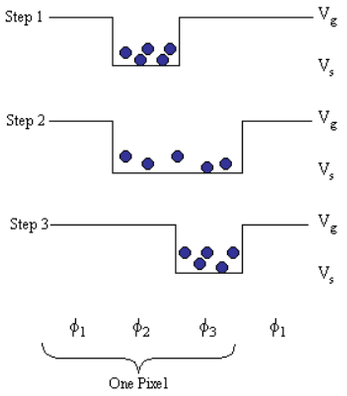












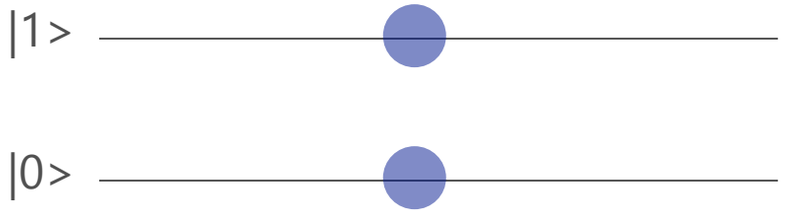
Oscillating Electric Field

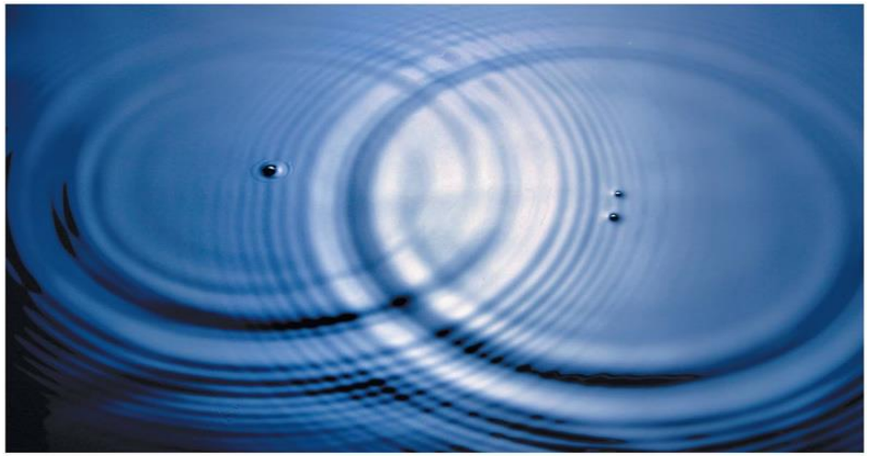
Oscillating Magnetic Field

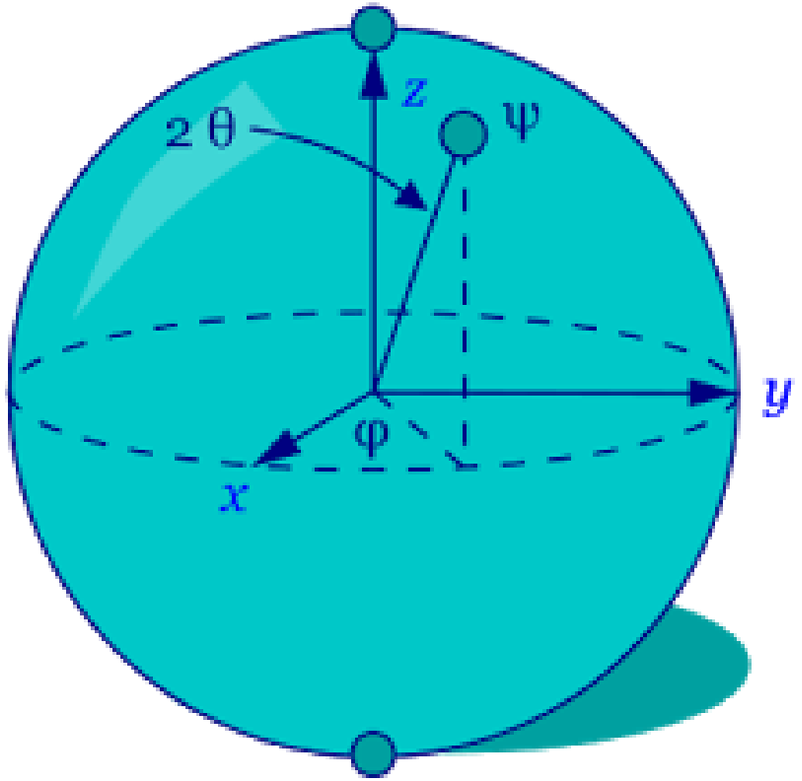
Laser Light

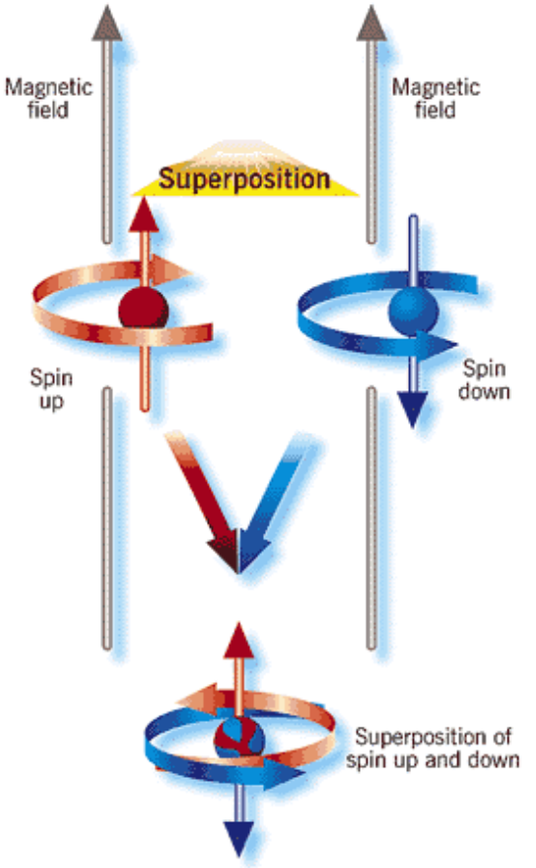
Path of quasiparticle

Quantum Superposition

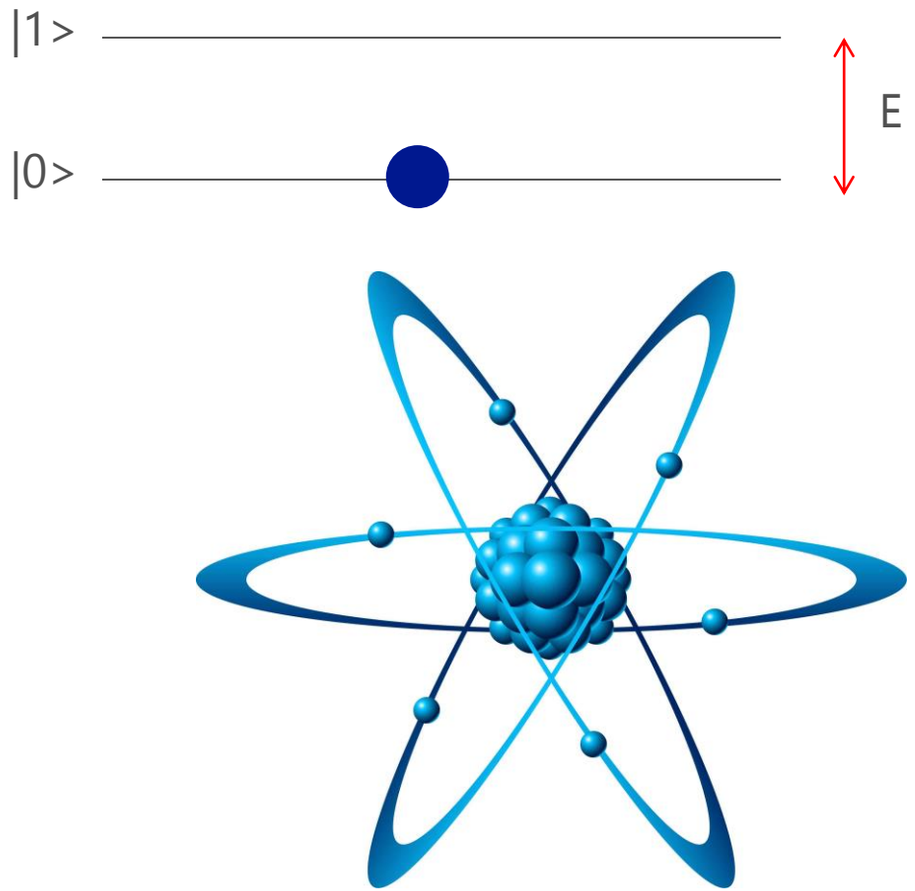








Quantum Readout



?

|1>

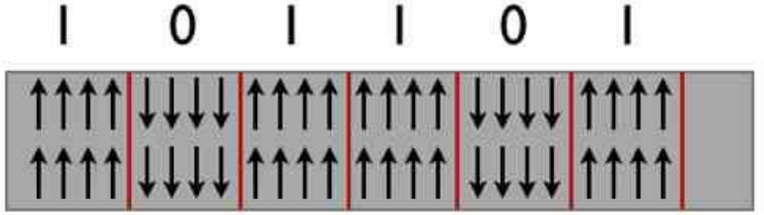
|0>

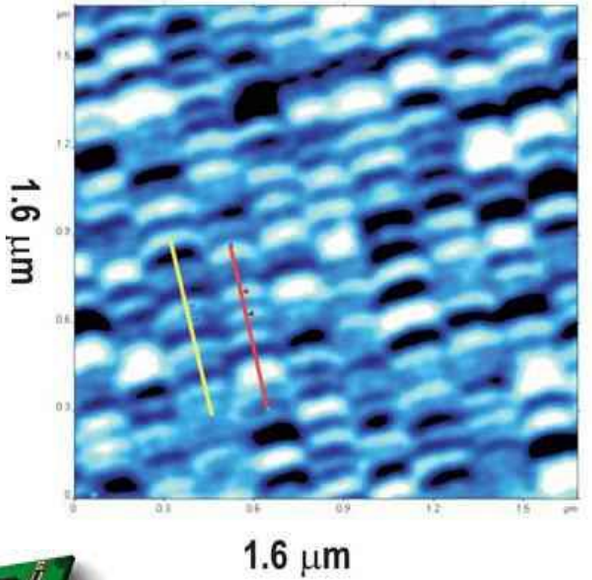
?

|1>

|0>

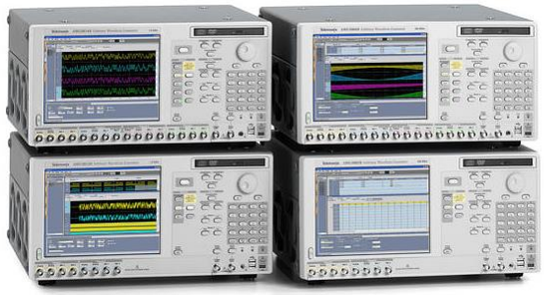
Manipulating Information

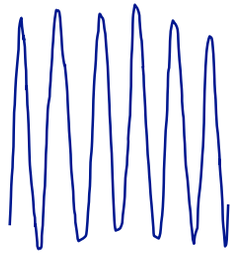




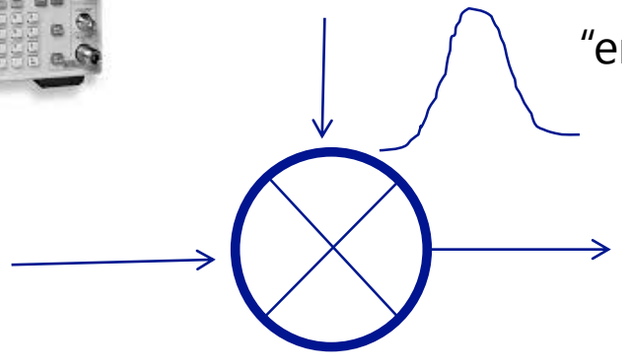
But quantum information is fragile
and in need of constant error correction
(a bit like DRAM)

Convergence of Control Technology

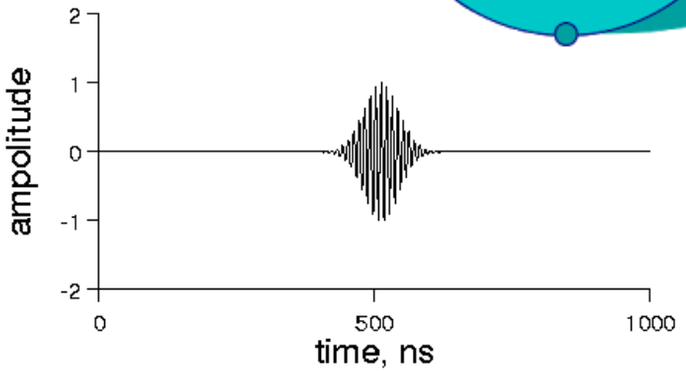


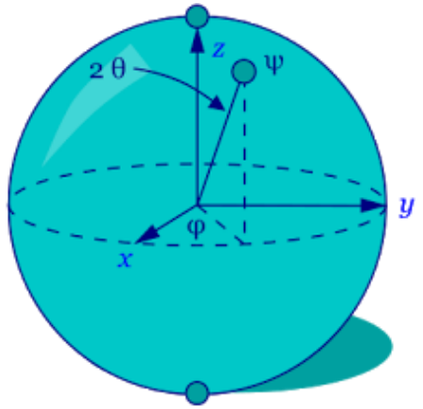


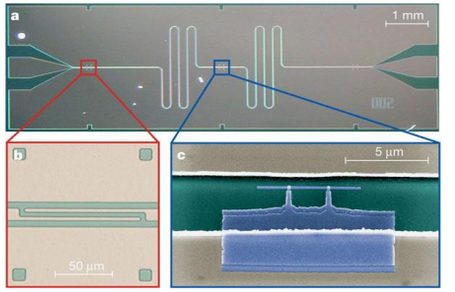
"carrier"

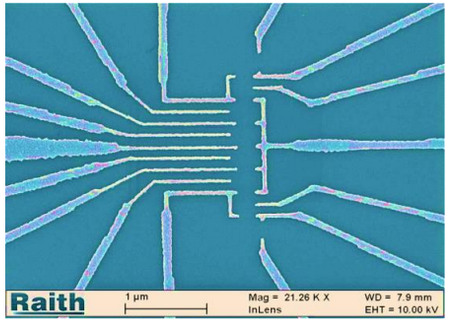


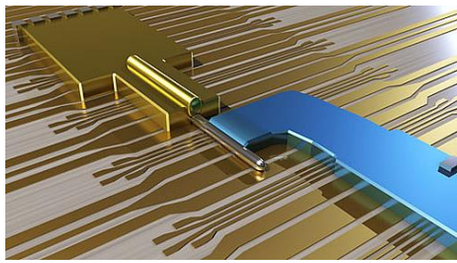
"envelop"





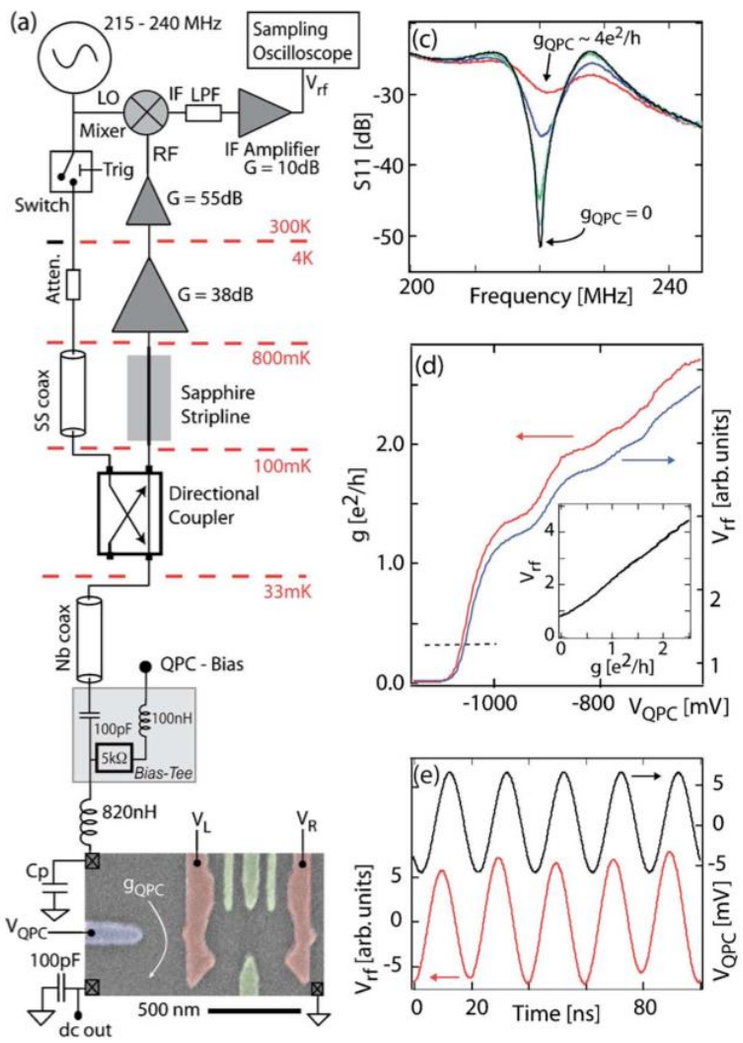


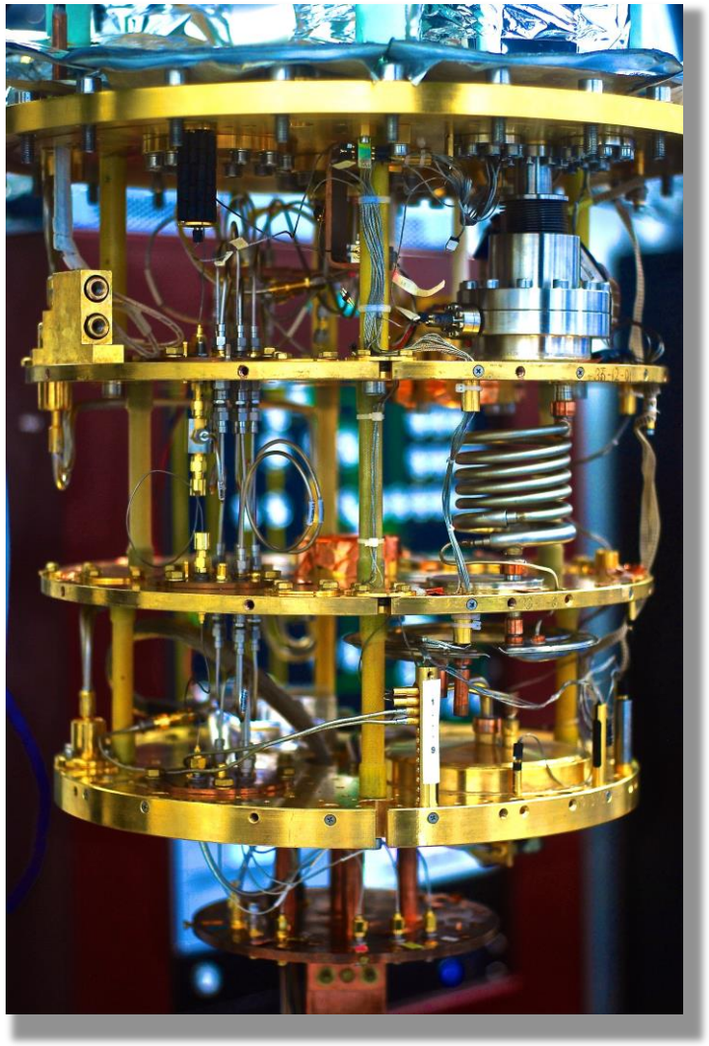


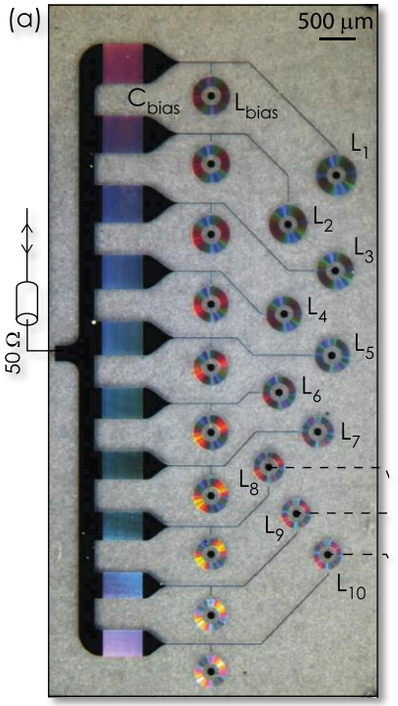


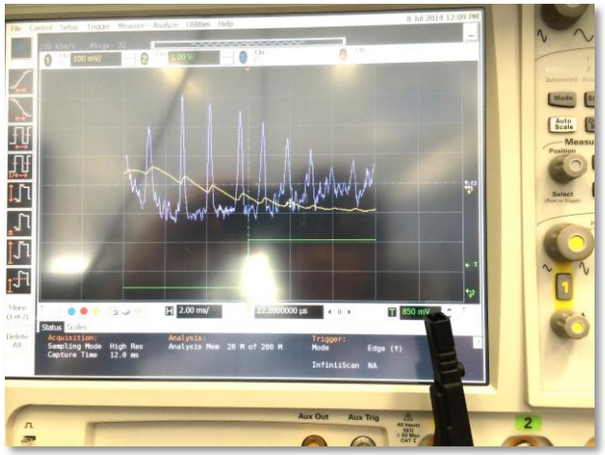
Width and amplitude of pulse sets "tip-angle"

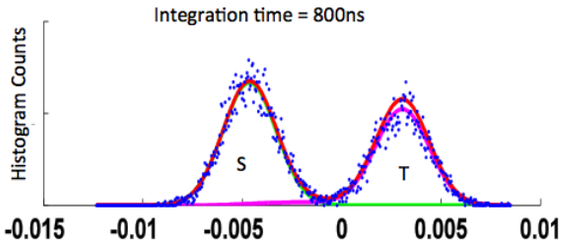
Convergence of Readout Technology



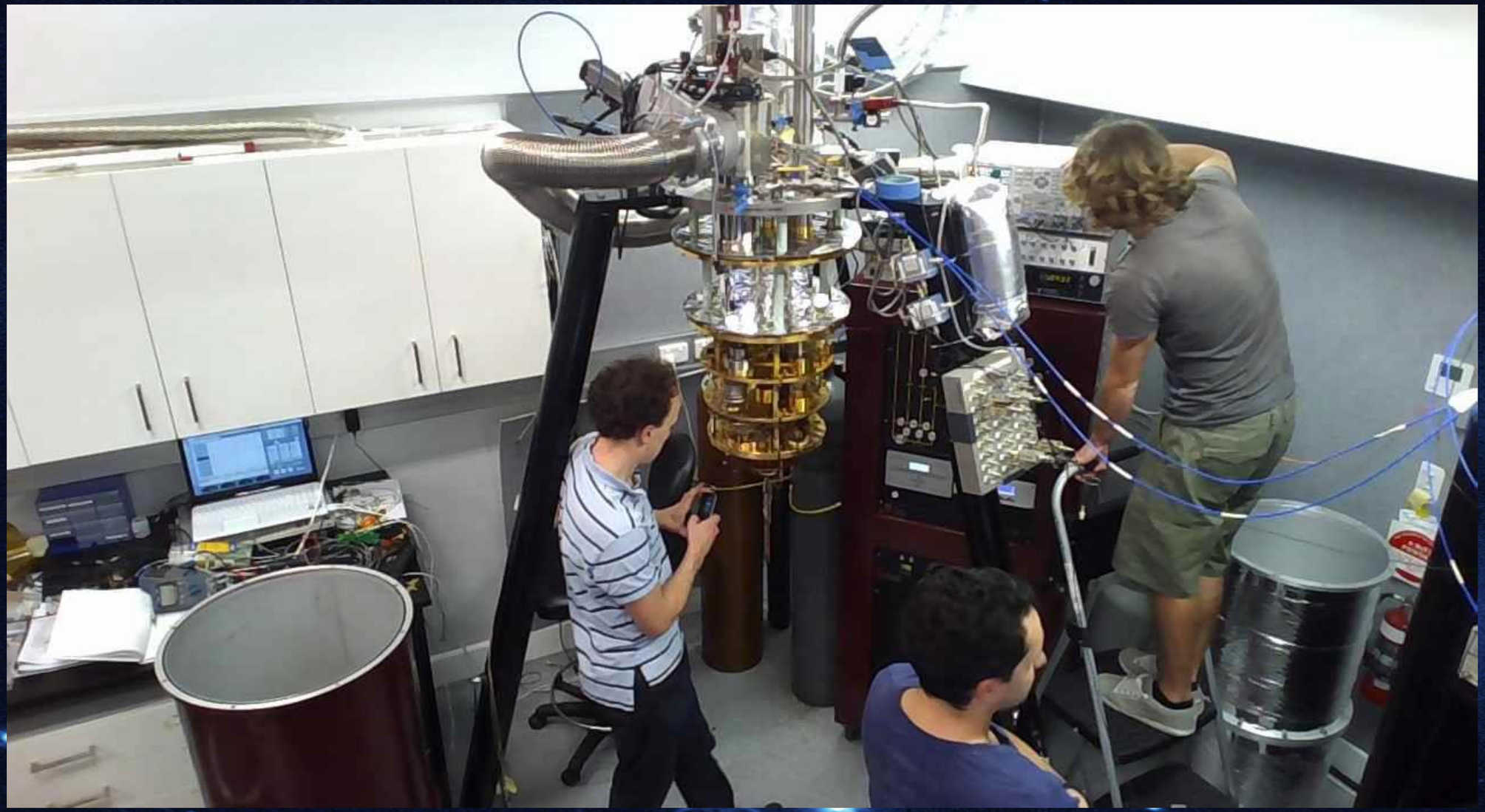




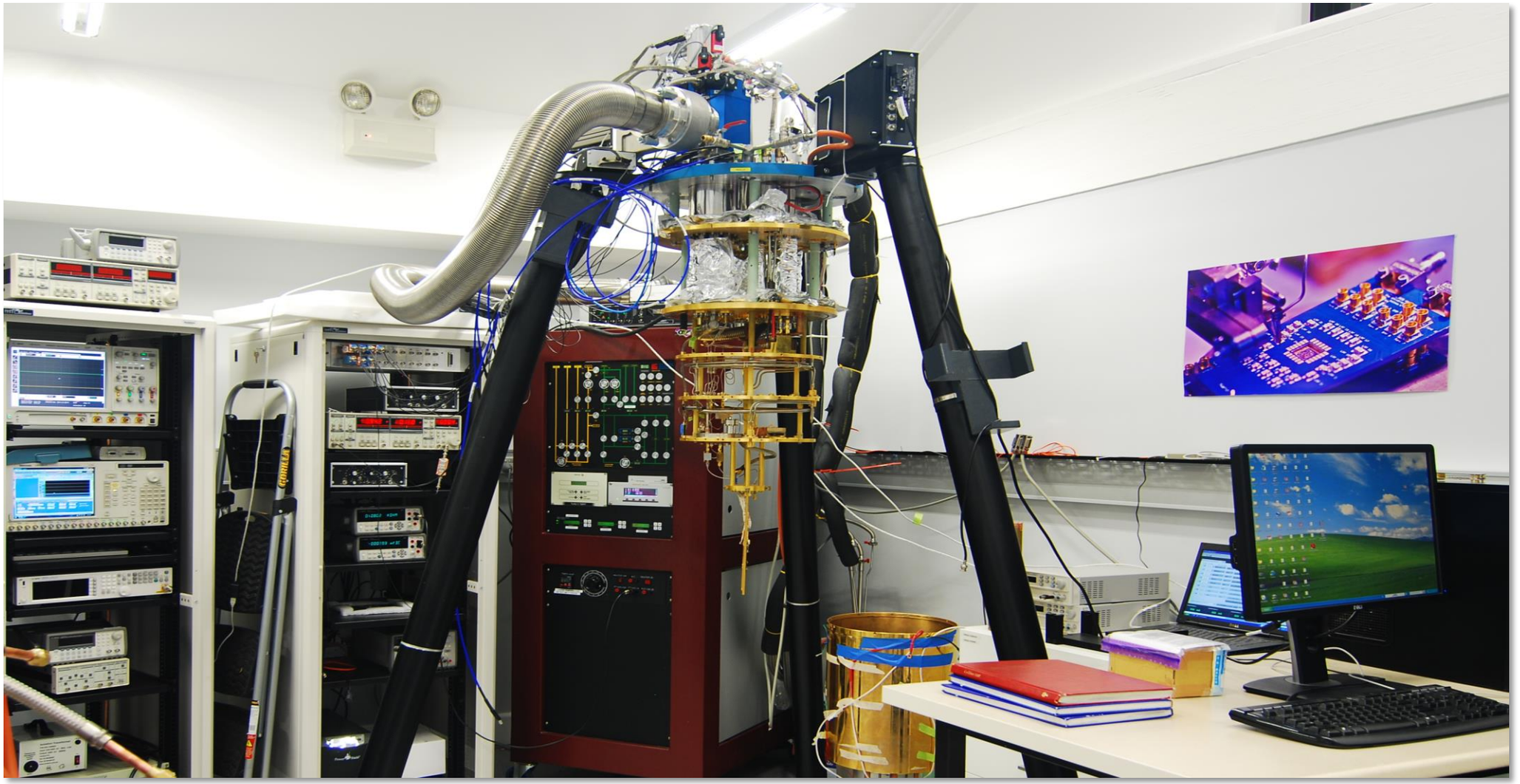




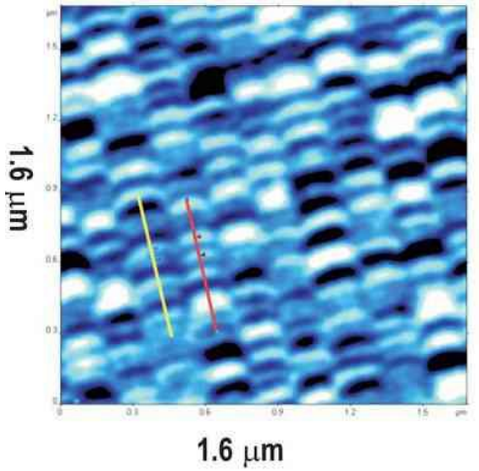
Colder than deep space



Footprint of 1 qubit



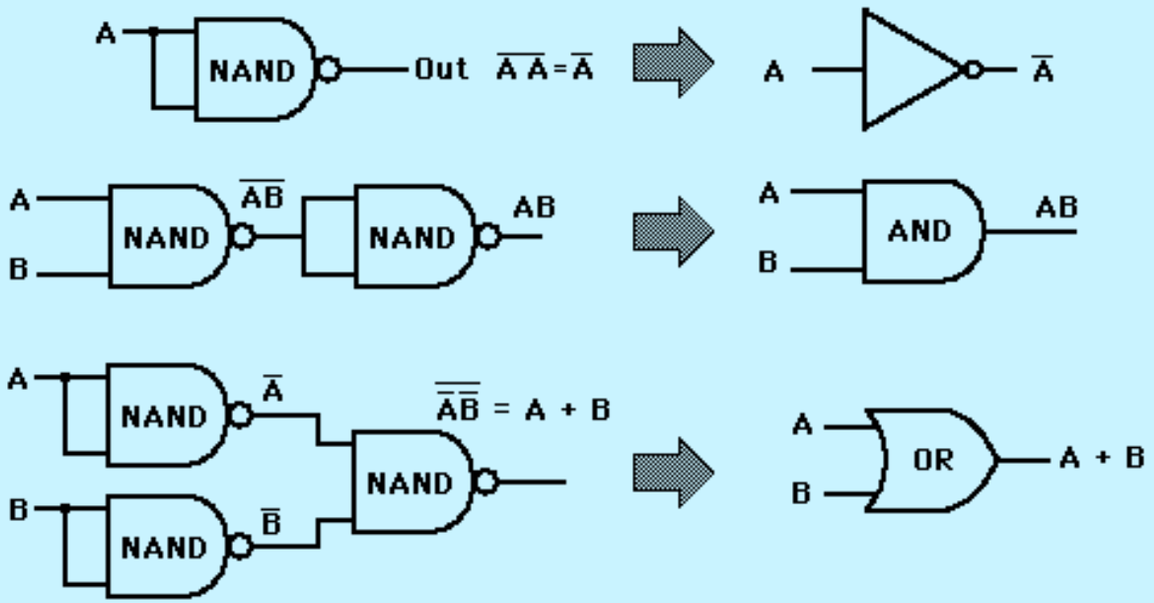
Read-Write Head for Every Domain?



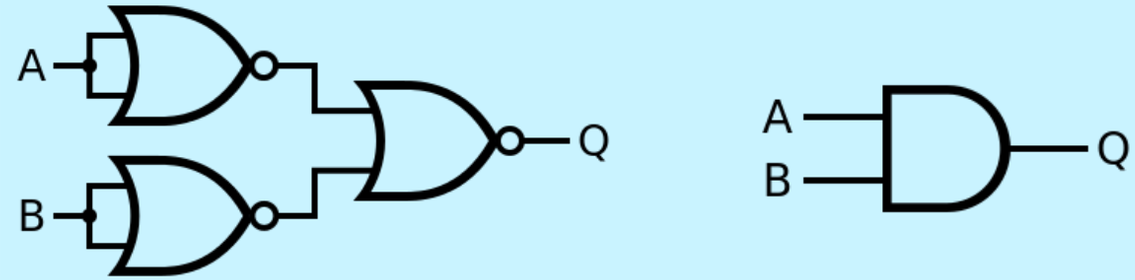
Need an approach that doesn't require fully parallel control and readout of every qubit

Universality

NAND gates are universal



NOR gates are universal



Set of Quantum Gates for Universal Computation

I — Pauli I (Identity) = $\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$

X — Pauli X (NOT) = $\begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$

Y — Pauli Y = $\begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}$

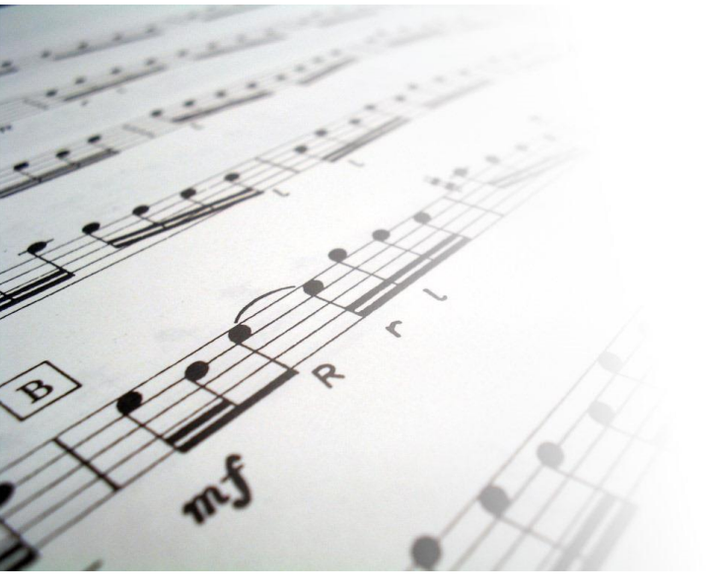
Z — Pauli Z (Phase Flip) = $\begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$

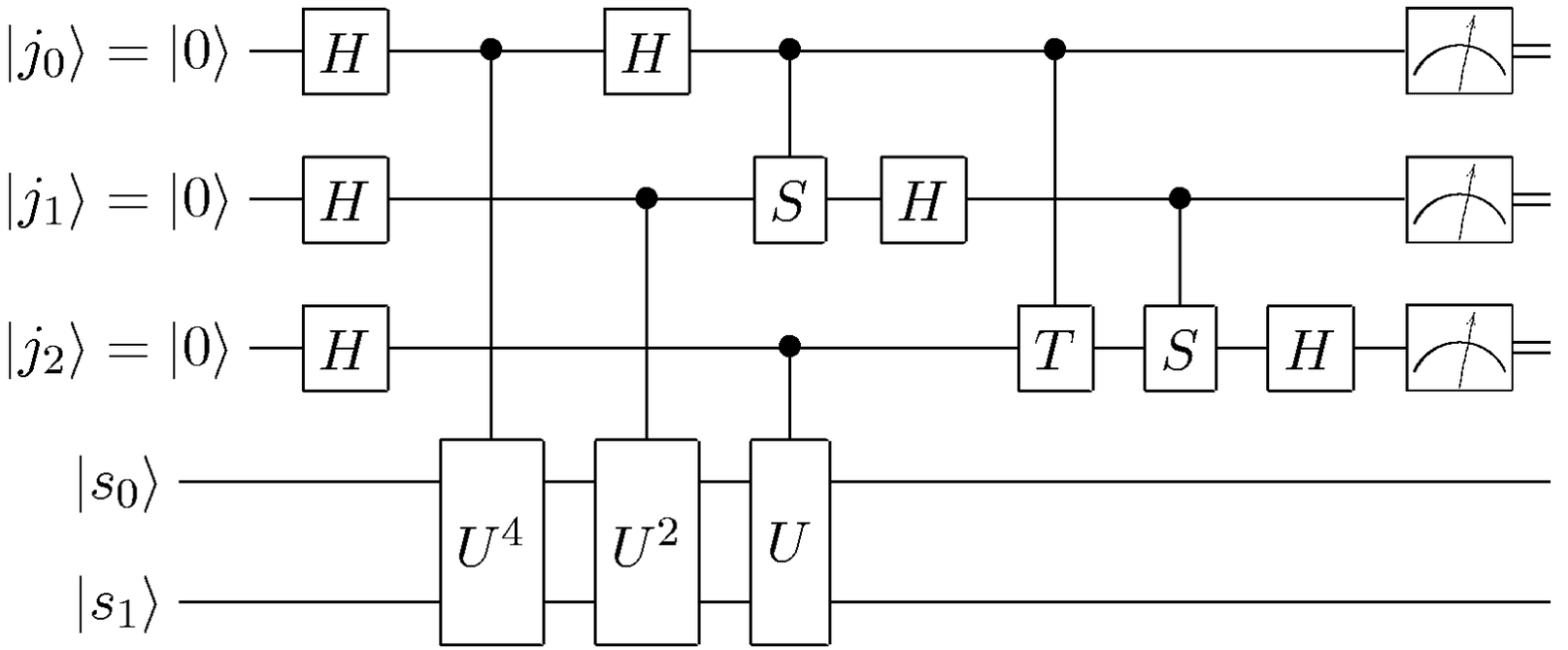
H — Hadamard = $\frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}$

S — Phase = $\begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix}$

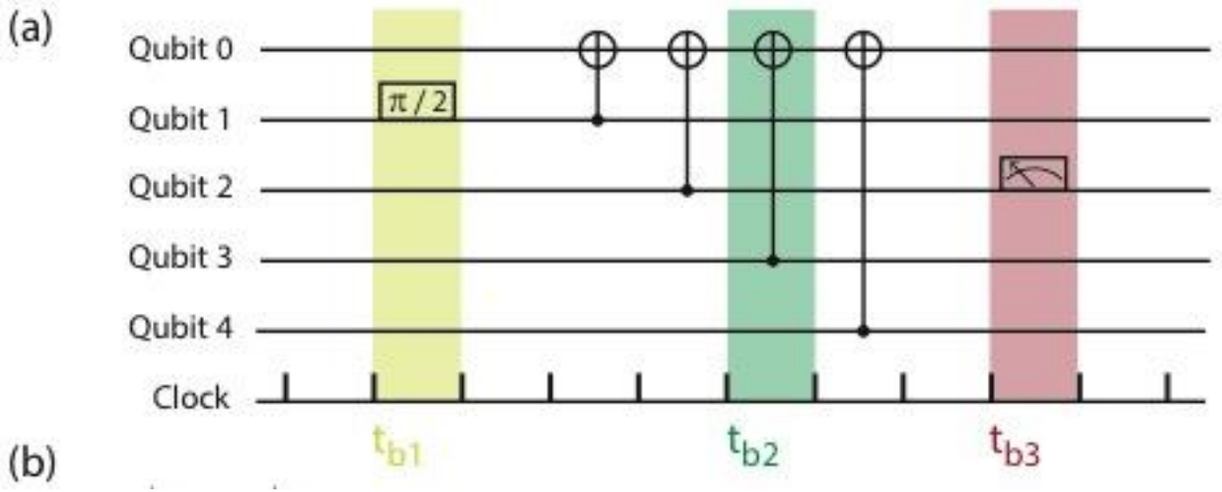
T — $\pi / 8 = \begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{pmatrix}$

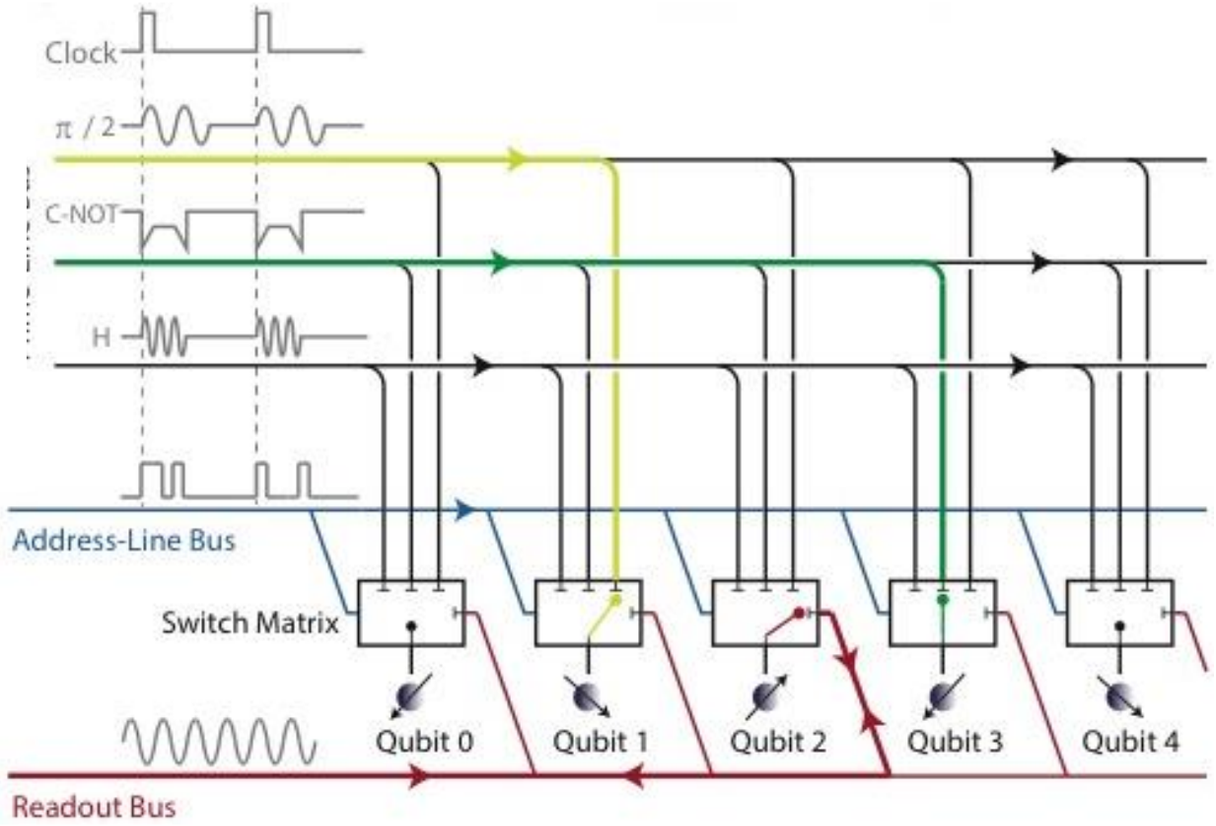
Circuit Model of Quantum Computation





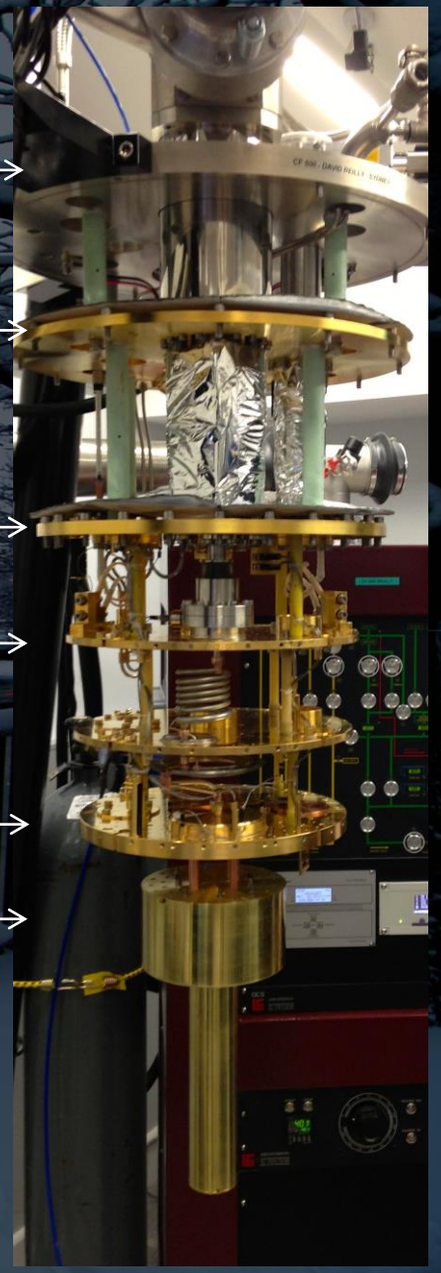
Separation of ‘prime waveforms’ and addressing





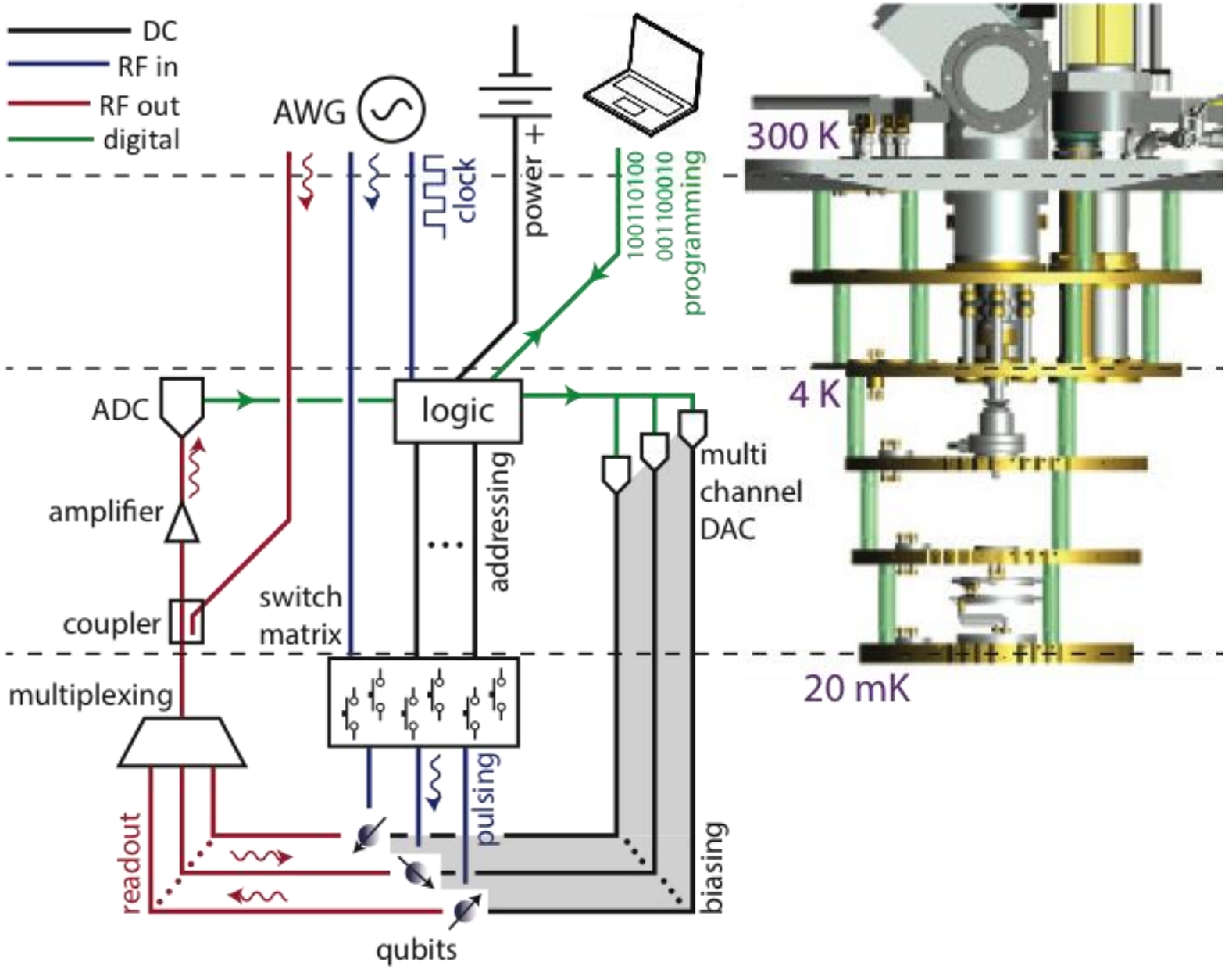
The need for cryogenic electronics

- Essential that switching array is cold, close to qubits.
- Benefits from locating logic and data converters in the cold:
  - Footprint, scaling
  - Superconducting Interconnects
  - Signal fidelity / bandwidth
  - Reduced latency
  - Noise performance
  - EMI
  - Enhanced clock speed



Cold Electronics

Superconducting
Transmission lines



Tomorrow's Solution

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Ultra-low-power superconductor logic

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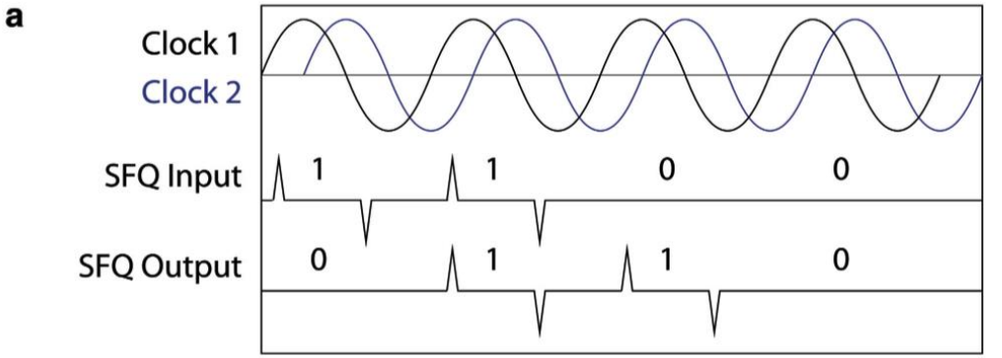
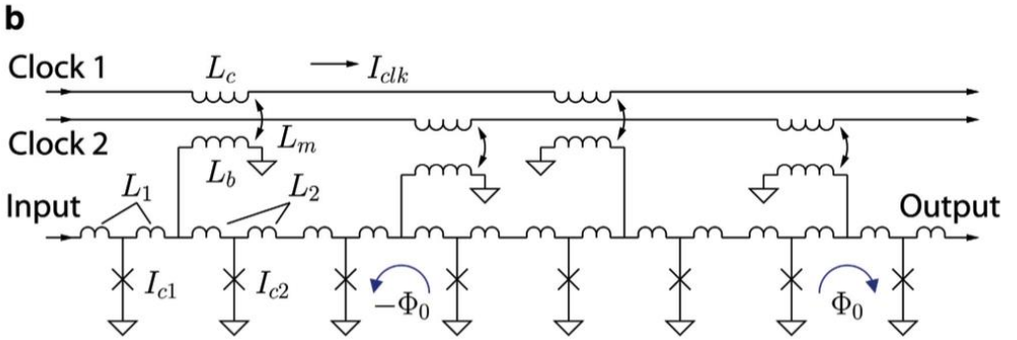
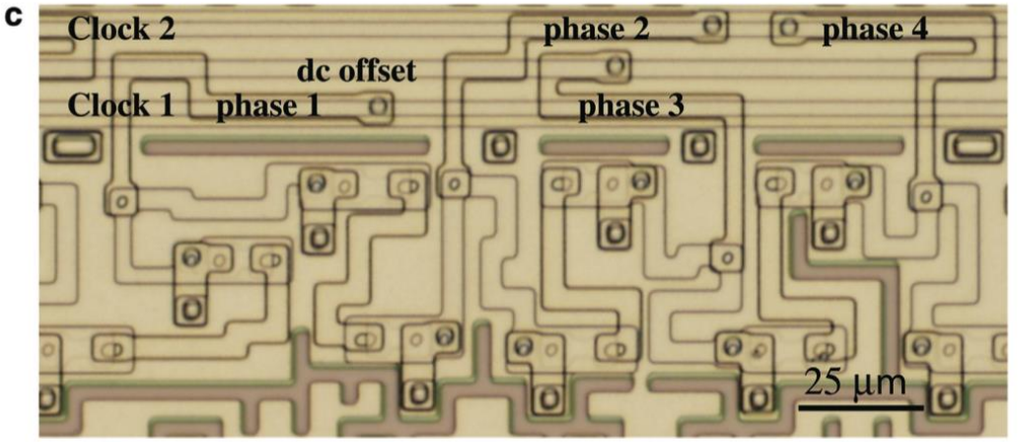
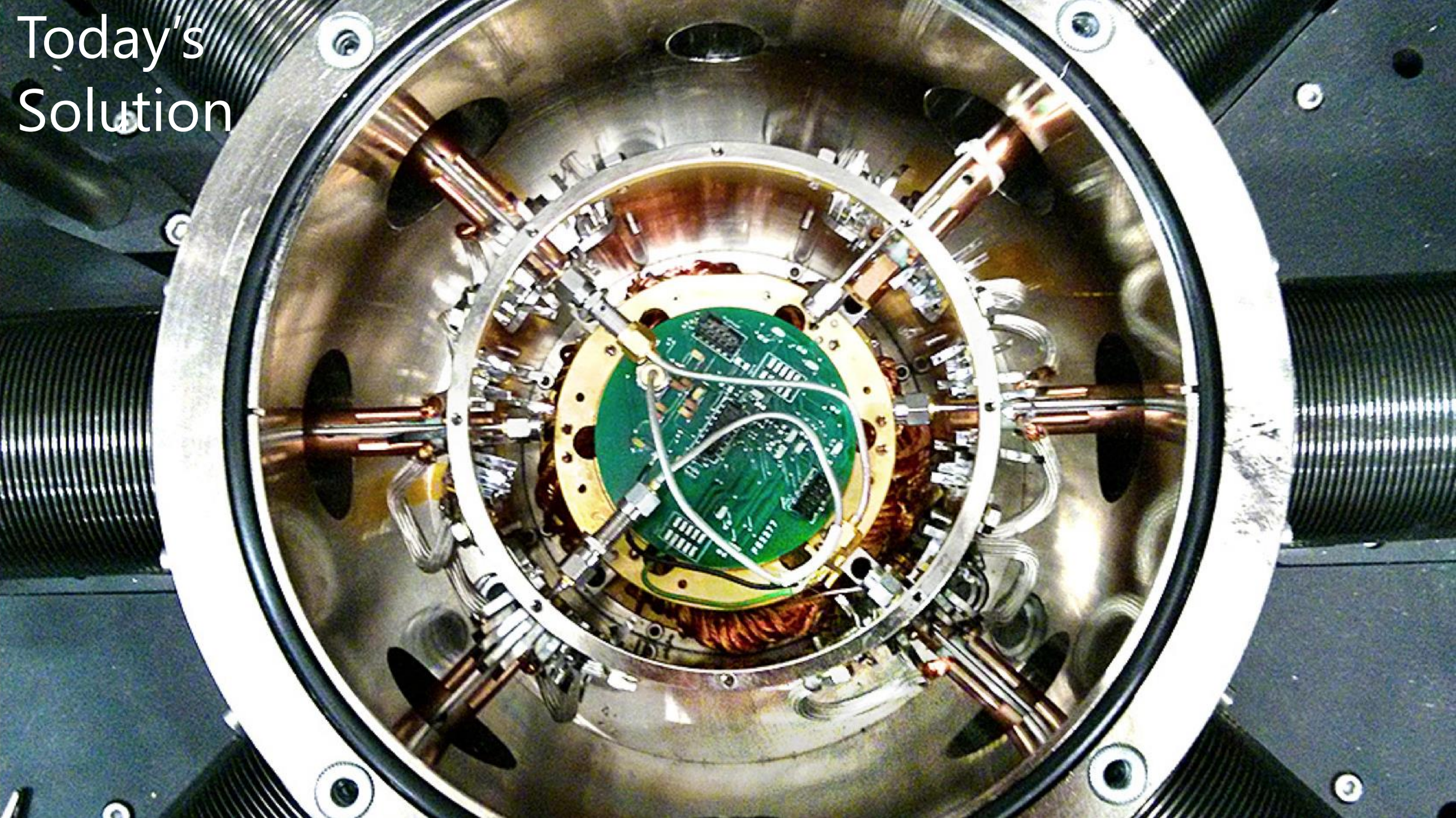
(Received 25 January 2011; accepted 31 March 2011; published online 17 May 2011)



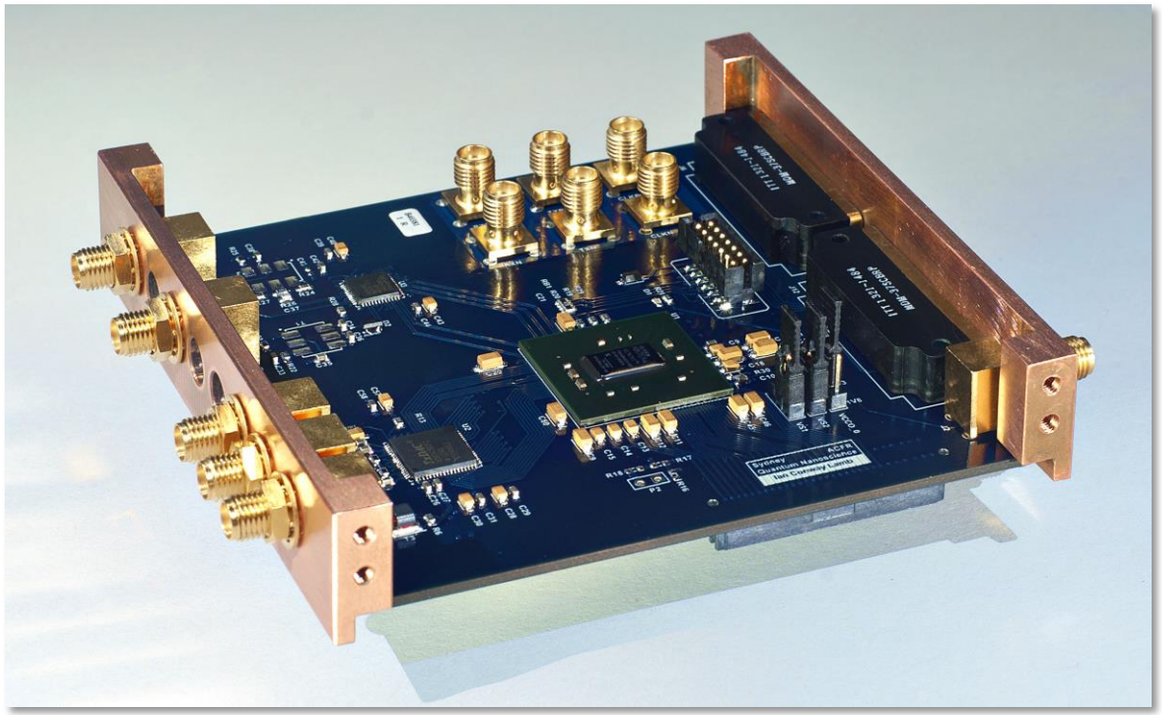


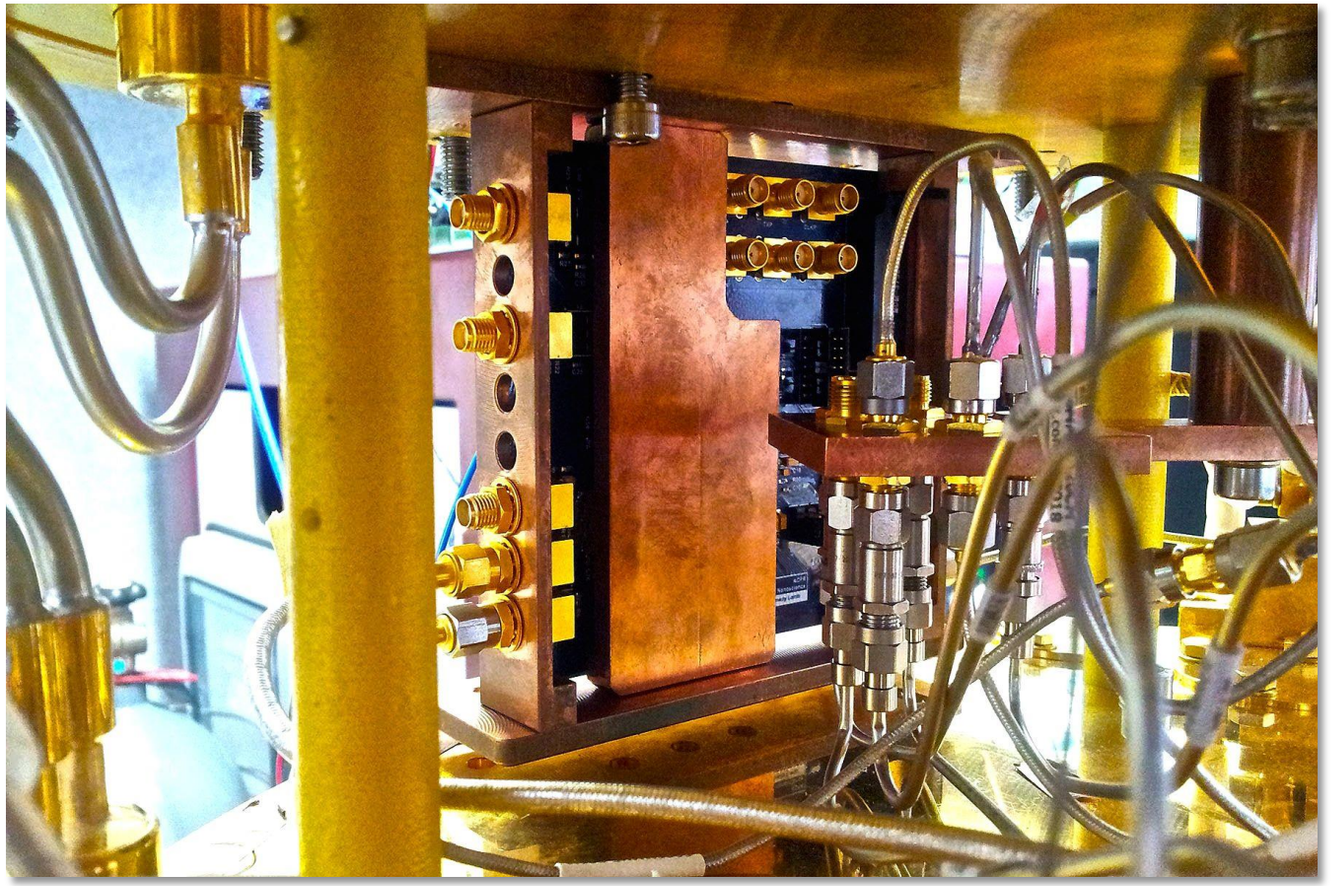


Today's Solution

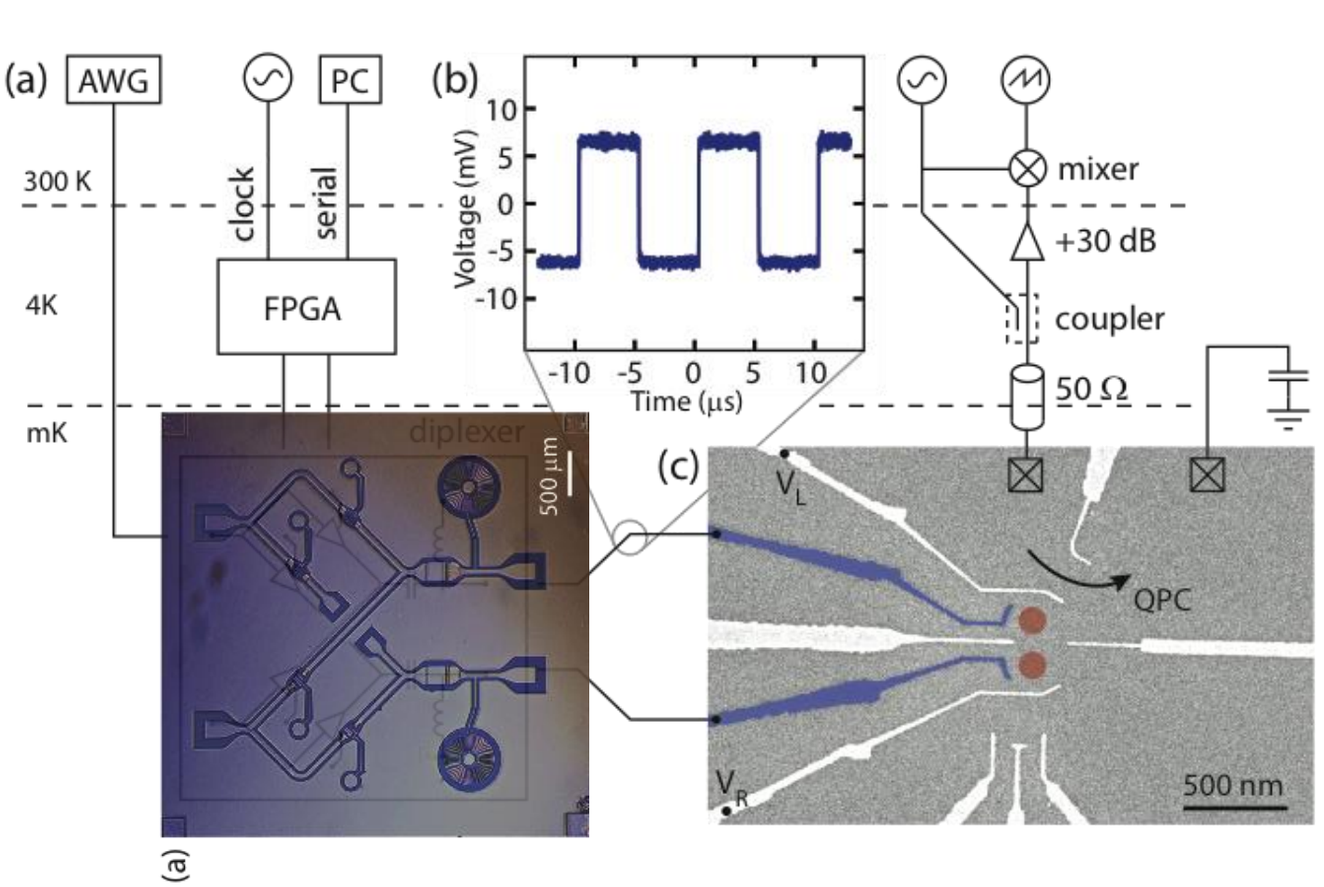


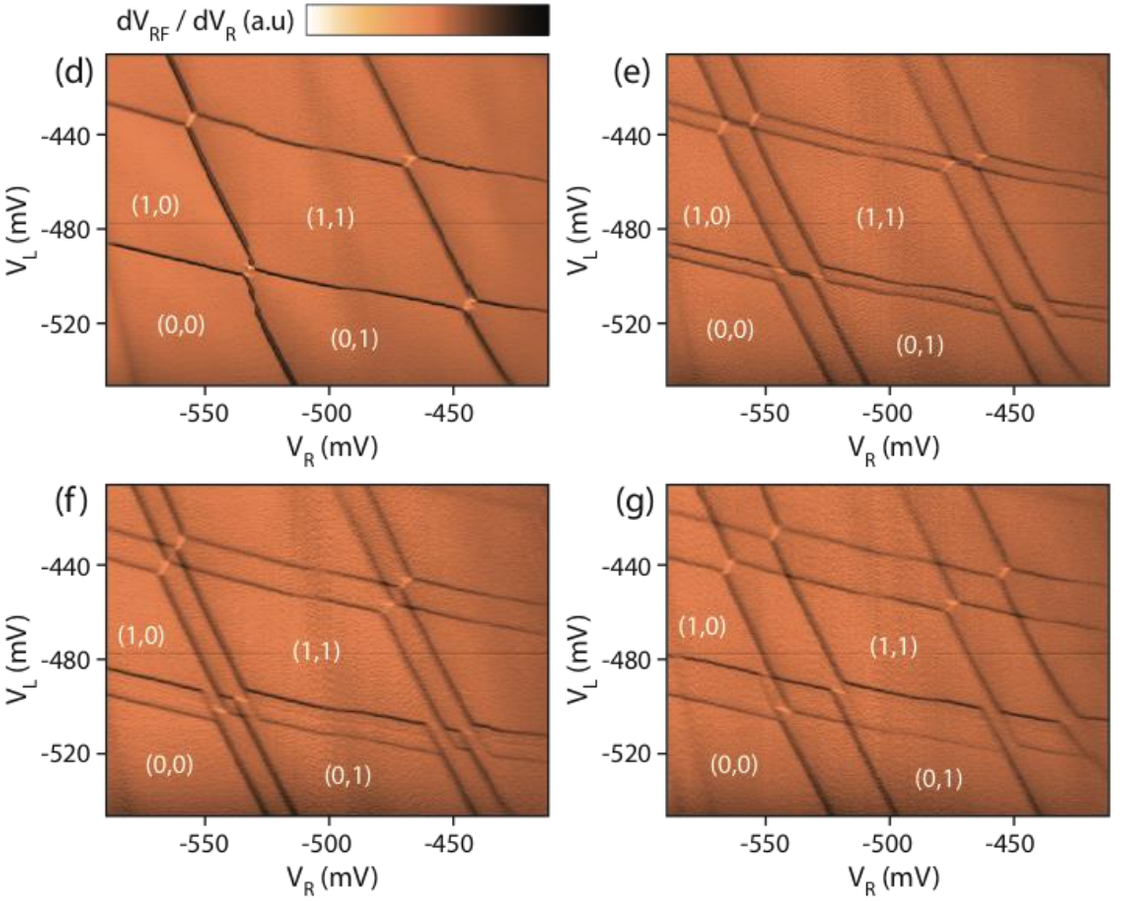
Fast Feedback in the Cold



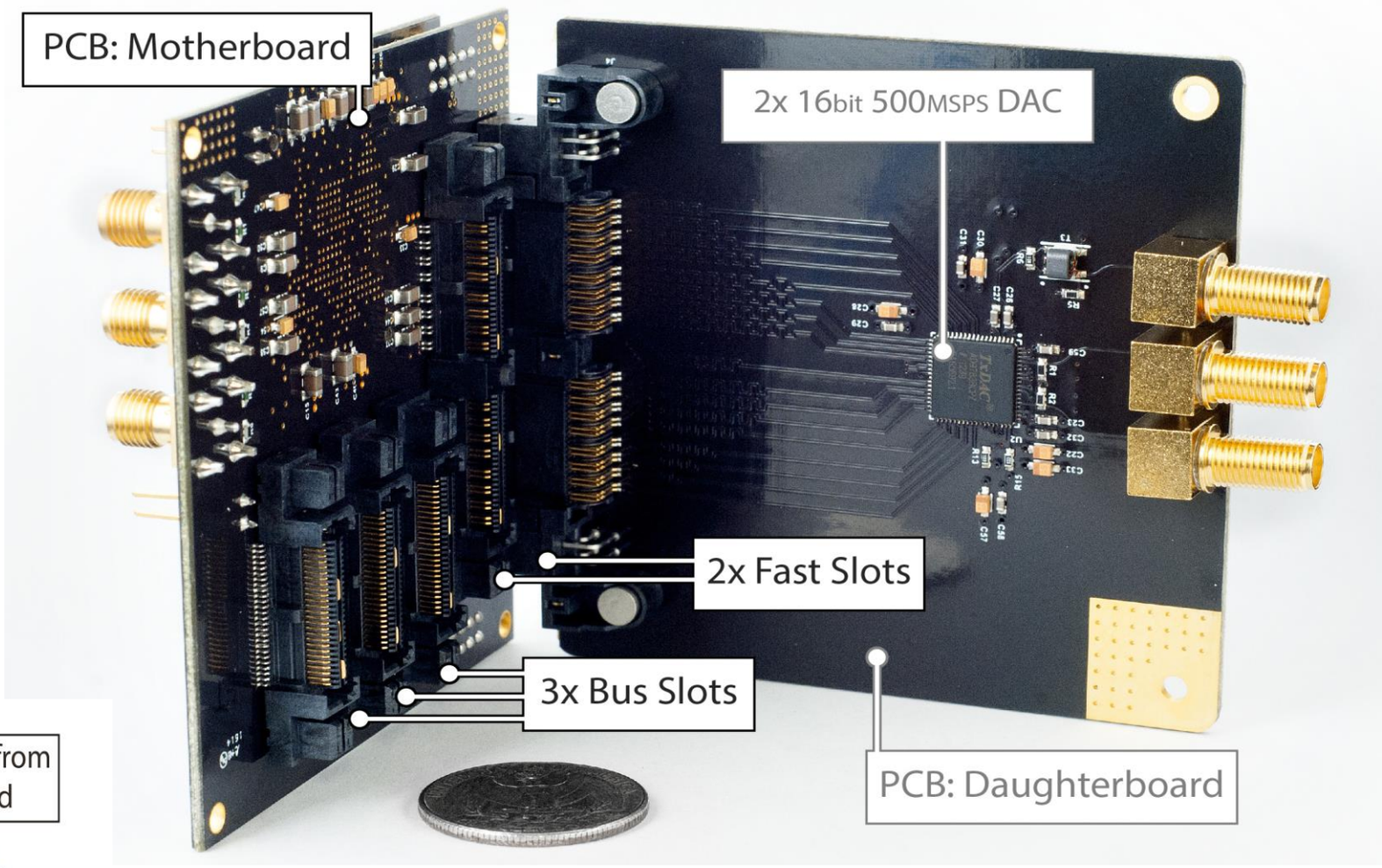


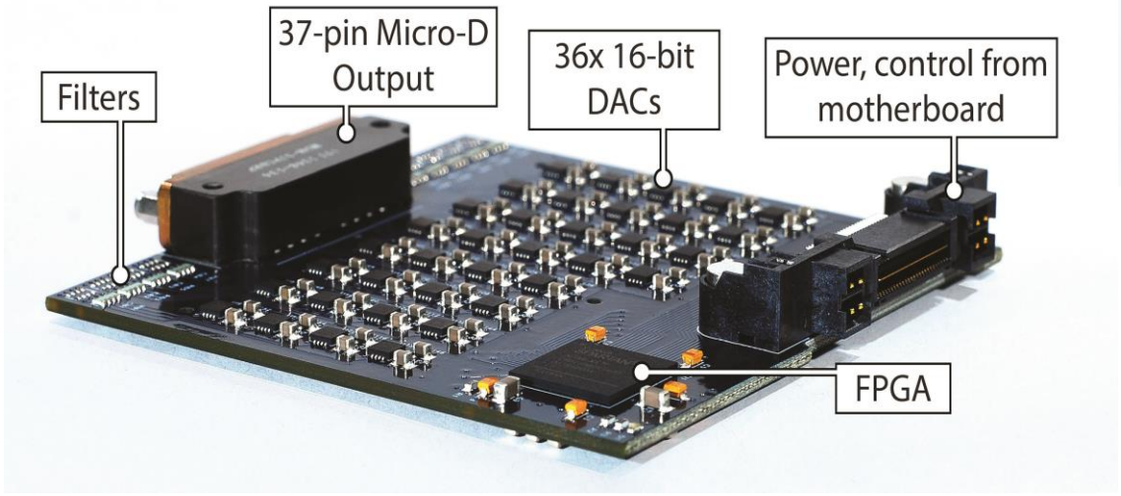
Cryo-FPGA, Switches, and Qubits Together…

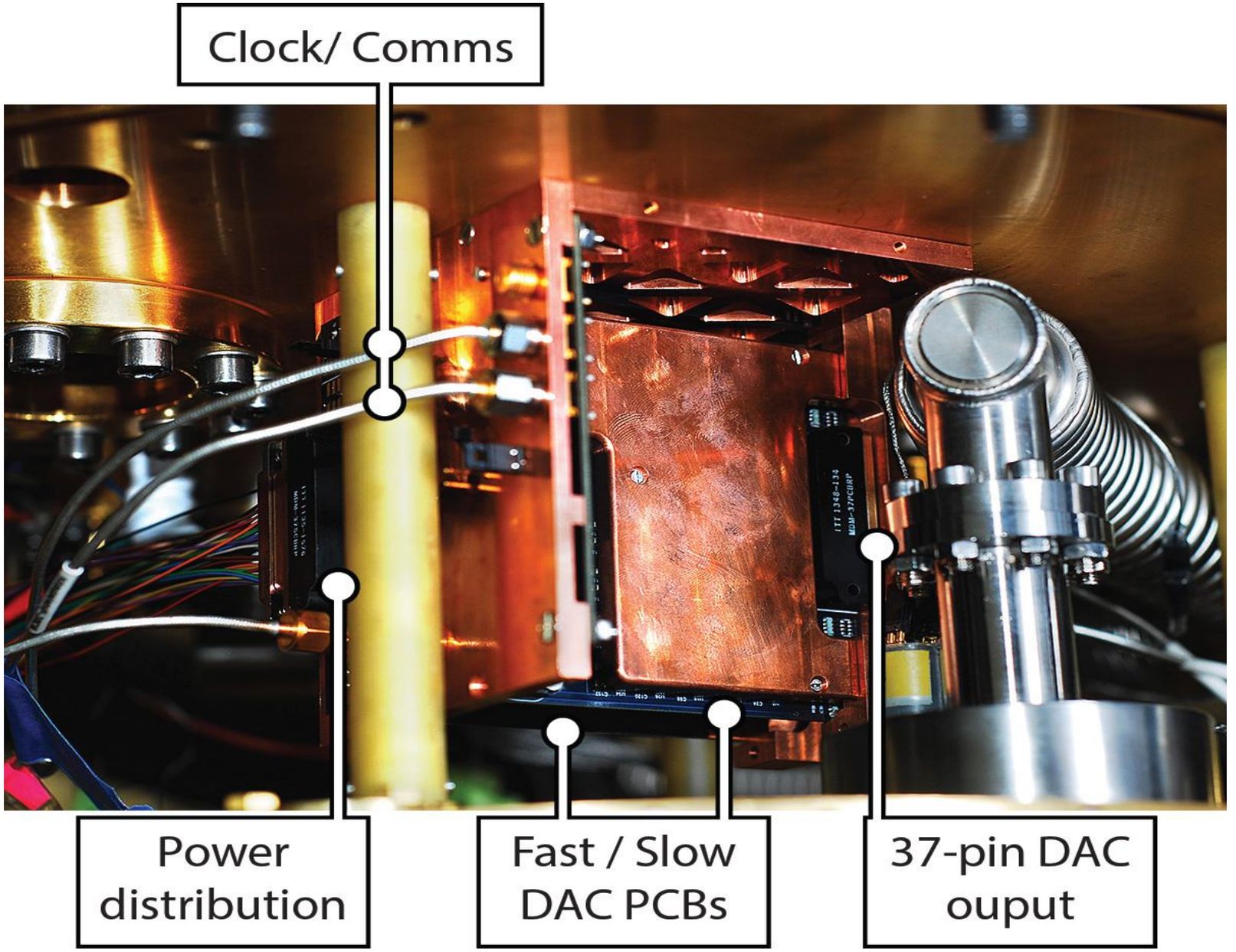




Next Steps…


PCB: Motherboard
2x 16bit 500MSPS DAC
2x Fast Slots
3x Bus Slots
PCB: Daughterboard


Filters
37-pin Micro-D Output
36x 16-bit DACs
Power, control from motherboard
FPGA


Clock/ Comms
Power distribution
Fast / Slow DAC PCBs
37-pin DAC ouput

Sydney Team

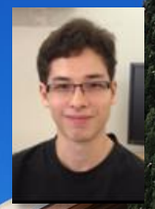

Alice Mahoney


Xanthe Croot


James Colless


Ian Conway-Lamb


John Hornibrook


Seb Pauka


Andrew Doherty


Philip Leong

eQus

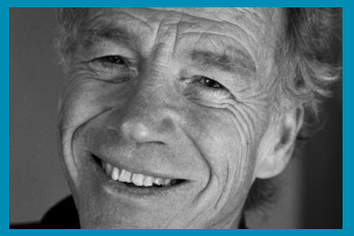
THE UNIVERSITY OF SYDNEY

Microsoft Research

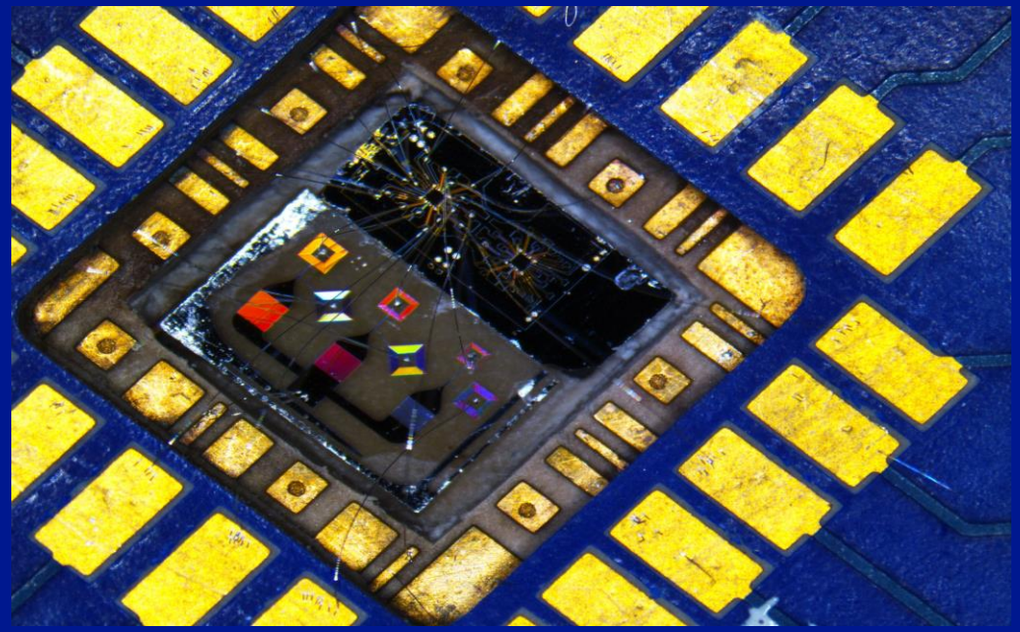

Burton Smith


Krysta Svore


Dave Wecker


Michael Freedman

Microsoft



15TH ANNUAL
Microsoft Research Faculty Summit 2014

Save the planet and return
your name badge before you
leave (on Tuesday)