On-chip Networks for FPGAs

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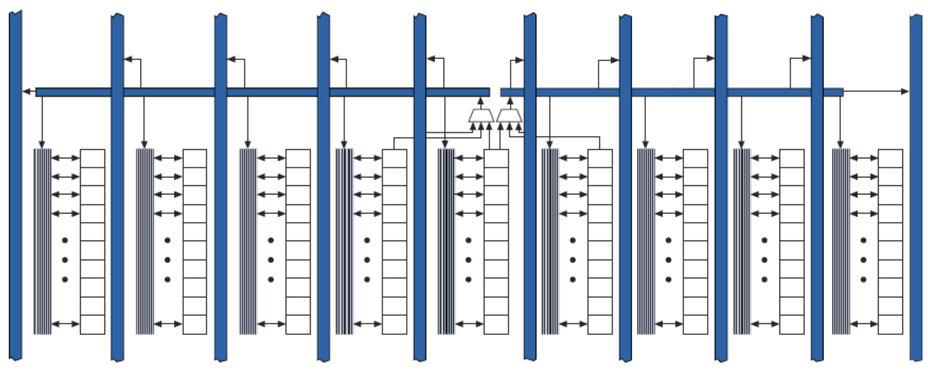
Overview

Field Programmable Gate Arrays combine configurable logic with configurable interconnect to implement increasingly complex systems. As systems scale the configurable interconnect demands more and more silicon resources. Networks-on-chip are emerging in the ASIC and multiprocessor world as an effective wire sharing and signal pipelining solution. The introduction of switched networks onto FPGAs is a necessary revolution that will radically change the way FPGAs are designed and used.



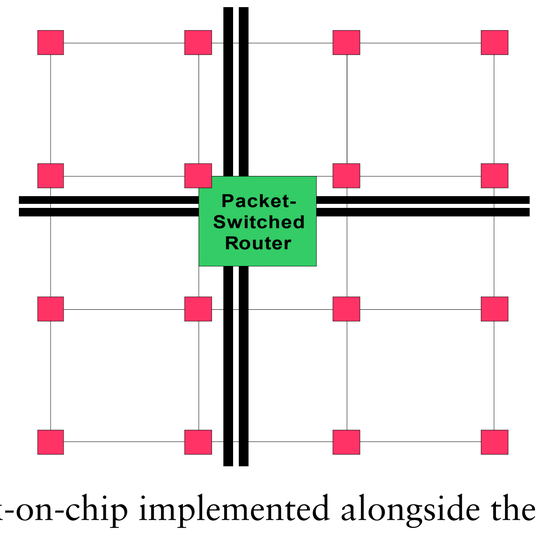
Stratix® Device FPGA logic elements and interconnect archtecture.
www.altera.com Stratix Device Handbook

Softcore vs. Hardcore

Softcore interconnect is implemented in the reconfigurable fabric. It is slow and resource hungry, but can be completely reconfigured in microseconds. A great deal of sacrifice is made for flexability.

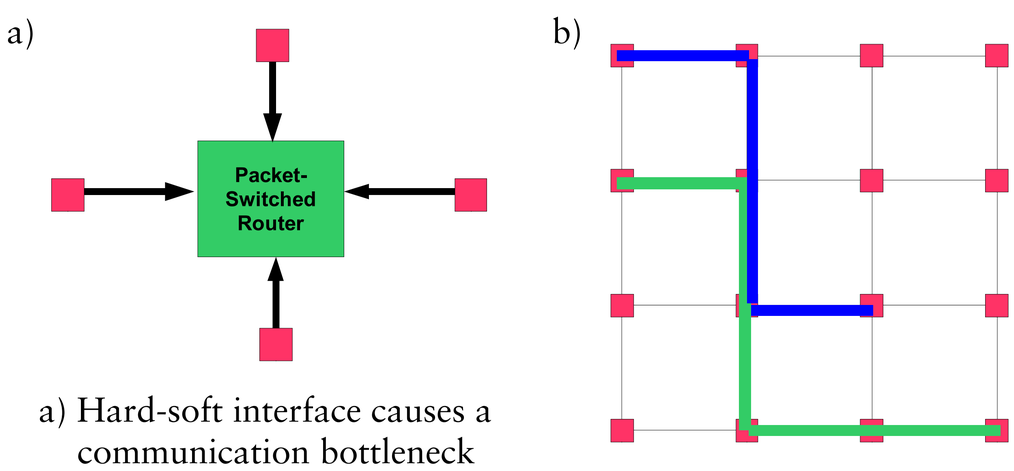
Hardcore interconnect is implimented in silicon alongside the FPGA fabric. It is fixed, but fast and small.

The aim is to redesign the FPGA so that the softcore systems can effectivly interface with hardcore interconnect.



Hardcore network-on-chip implemented alongside the FPGA logic elements

Wire sharing



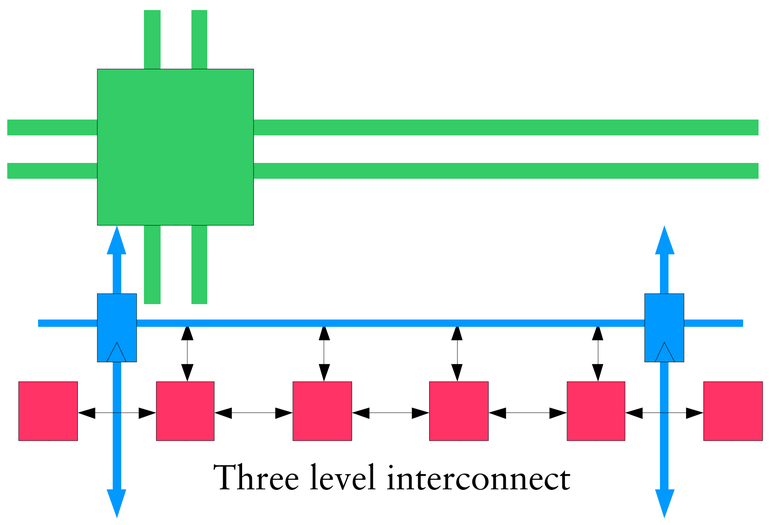
a) Hard-soft interface causes a communication bottleneck
b) Signal routes with wire sharing possibilities

Wire sharing allows greater FPGA density. We plan to replace the reconfigurable interconnect with a network that is fine-grained, high-speed and statically-scheduled.

A fine-grained network can also provide a high-speed interface to the hardcore packet-switched network-on-chip.

Wire sharing will be completely hidden from the system designer. Scheduling will be automated and performed after place and route. Developing a high performance scheduling algorithm is key to the success of this architecture and is the focus for this work.

Interconnect Hierachy



Three level interconnect

- Static bit-based local wiring will connect neighbouring logic elements.
- Statically scheduled bit-based shared wiring will seamlessly connect logic elements over medium distances at high speed.
- A dynamically scheduled nework-on-chip will connect high level soft- and hard-cores as well as transport data off-chip.

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